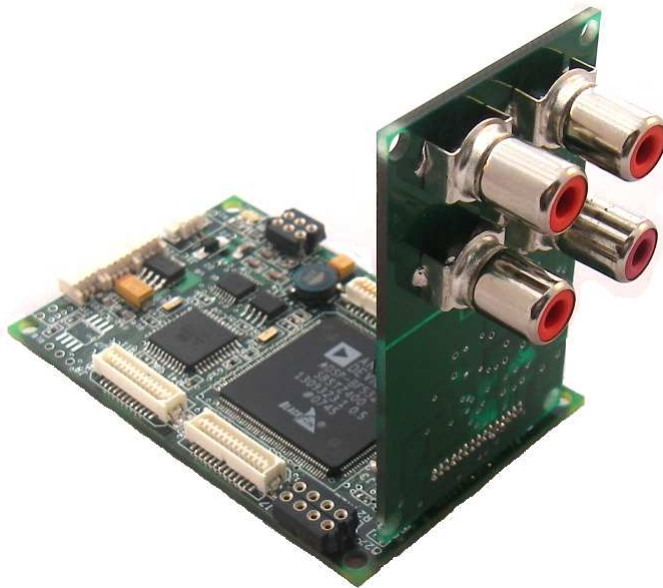S O C
R O B O T I C S

CM68   4 Channel NTSC/PAL Video Decoder

Technical Reference Guide
PCB Rev 1.0

www.soc-robotics.com

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Table of Contents

1.0 Introduction

Features:

- NTSC/PAL Analog Video Decoder
- One of four Video Input selection
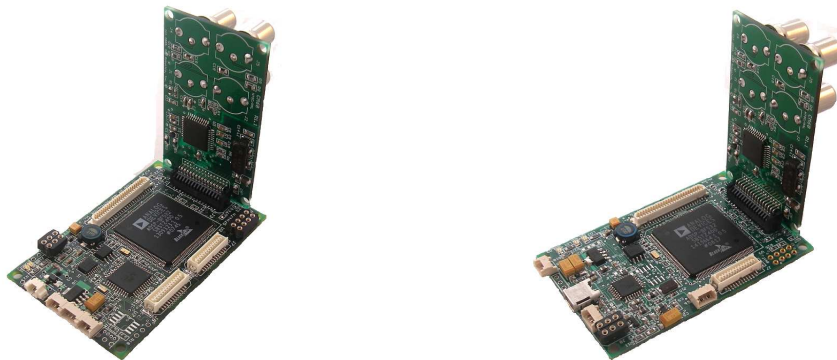- Attaches to P1 or P0 Blackfin DSP Board
- Automatically detect NTSC and PAL
- Video decoder is Philips SAA7113
- Programmed via I2C
- Outputs CCIR656 digital video stream
- Two different mounting options available
- Outputs YUV 4:2:2 video
- Extension I2C parameter setup
- 3.3V operation
- Dimensions: 1.50x2.50 inch
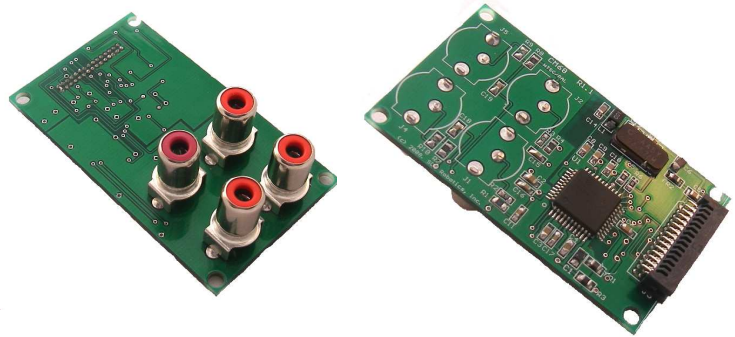
Hardware

The CM68 is a 4 Channel NTSC/PAL video decoder daughter card that attaches to the video input port of the P1 or P0 Blackfin embedded processing board. The CM68 automatically detects the presence of NTSC or PAL video signals and converts the analog video stream to digital YUV 4:2:2 output compatible with CCIR656 format. The onboard Philips SAA7113 video decoding chip is programmable and supports a wide selection of video encoding formats. See the Philips SAA7113 datasheet for detailed technical information on the chip. The P1 Boot Monitor includes complete source code to setup and configure the CM68 for real time DMA transfer of video to SDRAM.

The CM68 attached to the P1 and P0 Blackfin DSP boards.

Software

The CM68 is programmedby sending commands to the SAA7113 via an I2C bus. The P1 or P0 is provided with a Boot Monitor application that sets up the CM68 by loading the correct parameters into the SAA7113 registers. The P1/P0 Blackfin is programmed in C using either a Blackfin GNU C Compiler or the Analog Devices VisualDSP 4.5 Windows desktop C Compiler IDE. Complete source code for the CM68 setup procedure is provided. The P1/P0 Boot Monitor programs the CM68 and setups a real time DMA transfer of video data to SDRAM.

The example Project files that come with the CM68 were written using the Analog Devices VisualDSP Windows IDE. VisualDSP is a time limited free C development tool chain for the Blackfin DSP.

2.0 CM68 Detailed Description

2.1 Introduction

The CM68 is a four channel analog to digital video decoder daughter card for the P1/P0 Blackfin DSP boards. The CM68 decode NTSC and PAL analog video signals and outputs a CCIR 656 digital video stream with YUV 4:2:2 coding. The video decoding chip is the Philips SAA7113.
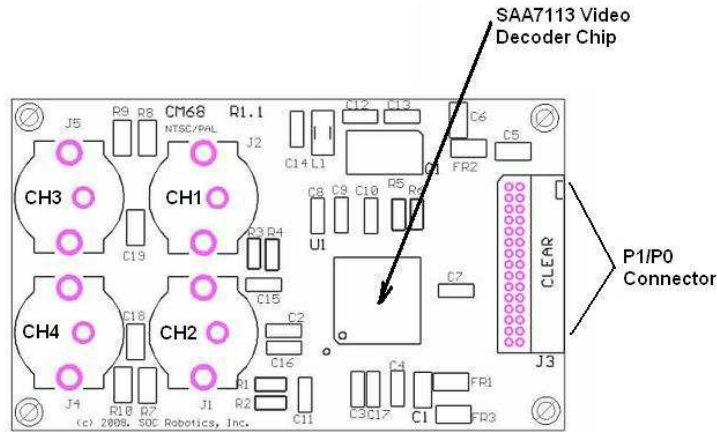
2.2 Video Decoder

The CM68 video decoding chip is the Philips SAA7113. The SAA7113 is configured by sending commands to it on its I2C interface. The chip is capable of automatically detecting the video encoding as NTSC or PAL with many different encoding variations. Refer to the SAA7113 datasheet for detailed technical information. The CM68 SAA7113 chip is programmed by sending commands to it via the I2C signal lines on connector J3. Two signals on the video output port connector are actually I2C lines. Default write address is 0x4A and default read address is 0x4B.

2.3 Video Input Ports

The CM68 has four analog video input ports only one of which is active at any given time. The active video port is selected under software control by sending the appropriate selection signal to the SAA7113 via the I2C interface.

2.4 P1/P0 Connector Interface

The CM68 attaches to the P1/P0 on connector J3. The pin assignment for J3 is shown below with P1 pin mapping.
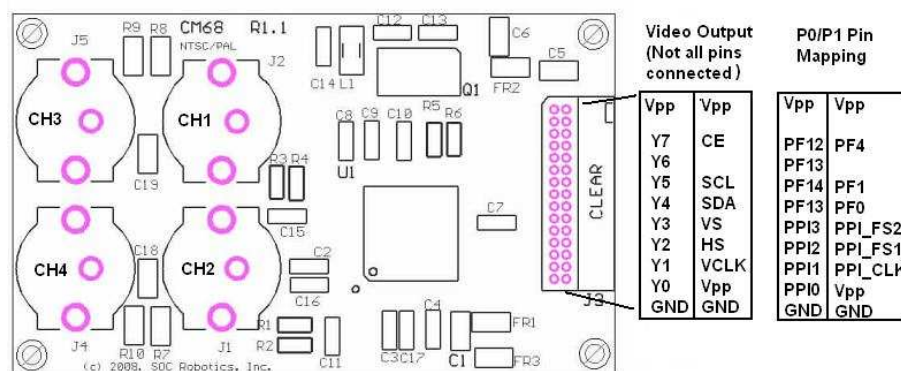
3.0 Software and Applications

3.1 Introduction
The CM68 is a software programmed video decoder that must be initialized before use. The SAA7113 datasheet describes the mapping between chip functions and I2C commands. The Blackfin Boot Monitor implements a complete configuration setup of the SAA7113. See the Boot Monitor source code for a detailed description of the command setup.

3.2 Application Description for P1
The application example that sets up the CM68 in the P1 Boot Monitor sets the SAA7113 default parameters, programs the DMA subsystem, sets all PPI pins to the correct setting and starts the DMA engine transferring decoded video to SDRAM. The user can select color or black and white and the video input channel. The application example is setup to handle NTSC decoded video streams. A different DMA configuration is required to handle PAL.
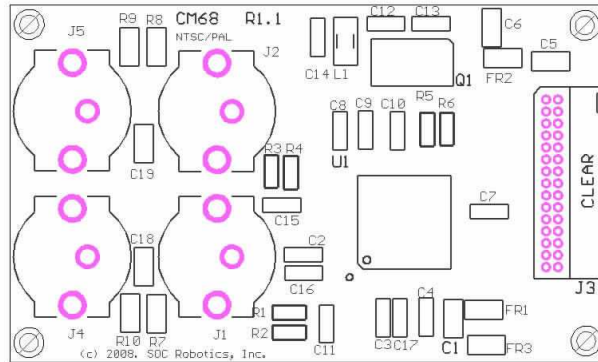
3.3 P0, P1 Processor Interaction
Blackfin (P0, P1) processor family can all control the CM68 via the I2C interface.

Electrical and Mechanical Description

Component Layout
Components are mounted on one side of the board.

Electrical Specifications
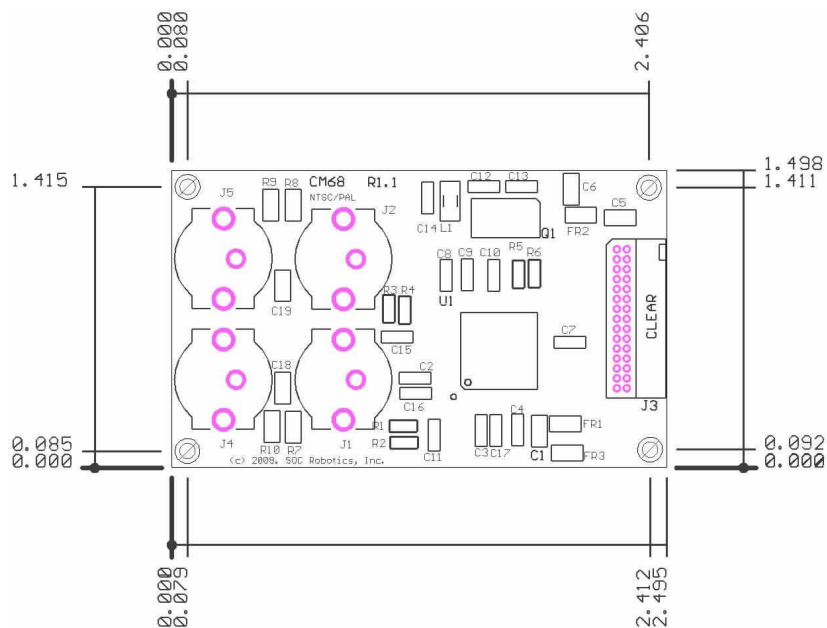
Electrical
Logic Power:　3.3VDC
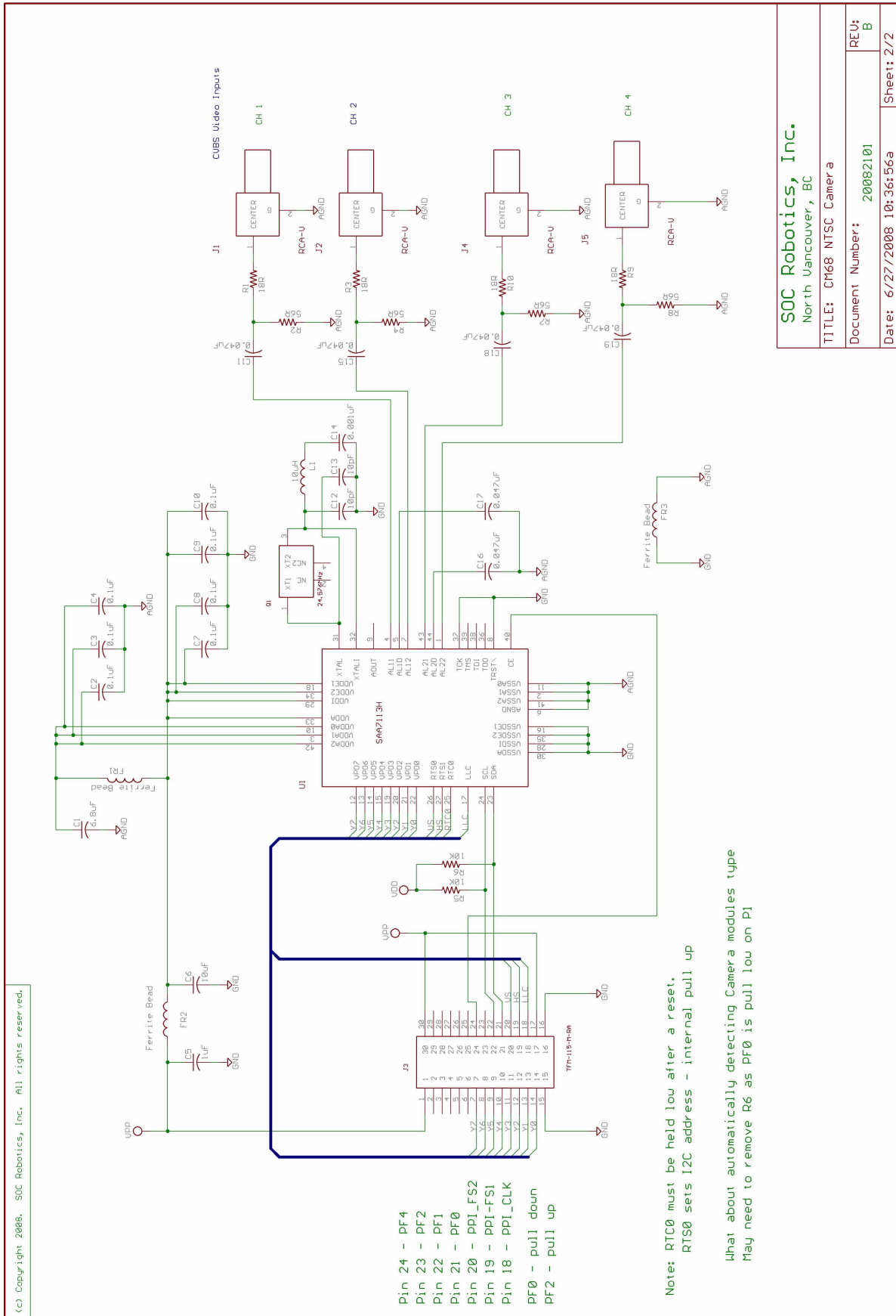
Mechanical
Dimensions:　2.50 x 1.50 in
Weight:　　　20 grams

Mechanical Dimensions
Board dimensions are stated in inches.

CM68 Circuit Schematic

NTSC/PAL Camera Module

CM68 4 Ch

PCB R1.1

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TITLE: CM68 NTSC Camera

Document Number: 20082101

Date: 6/27/2008 10:36:56a

REV: B

Sheet:1/2

Pin 24 - PF4
Pin 23 - PF2
Pin 22 - PF1
Pin 21 - PF0
Pin 20 - PPI_FS2
Pin 19 - PPI_FS1
Pin 18 - PPI_CLK

PF0 - pull down
PF2 - pull up

Note: RTC0 must be held low after a reset.
      RTS0 sets I2C address - internal pull up

What about automatically detecting Camera modules type
May need to remove R6 as PF0 is pull low on P1

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TITLE: CM68 NTSC Camera

Document Number: 20082101

Date: 6/27/2008 10:36:56a

REV: B

Sheet: 2/2

Notes: