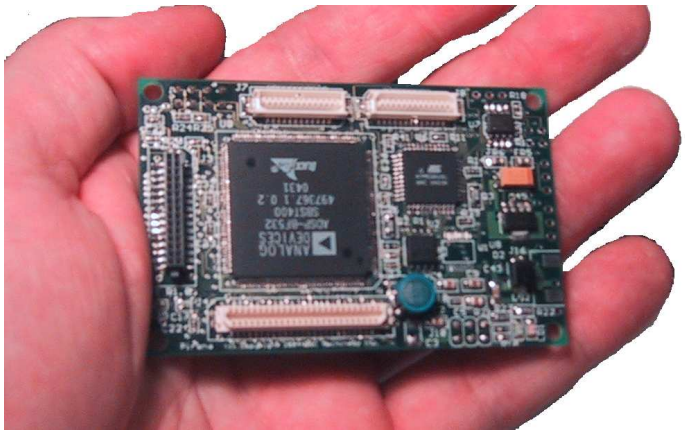
# P1 Pirana

## Smart Embedded Video Processor Hardware Reference Guide

PCB Rev 1.0b



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1935A–08/00/5M

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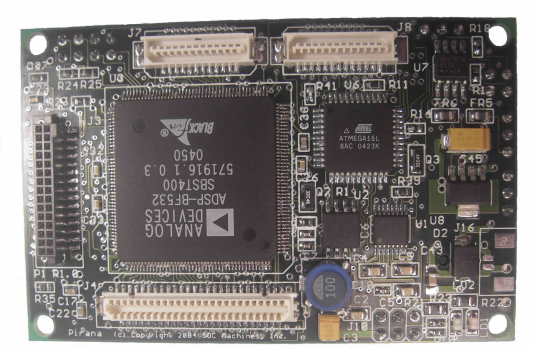
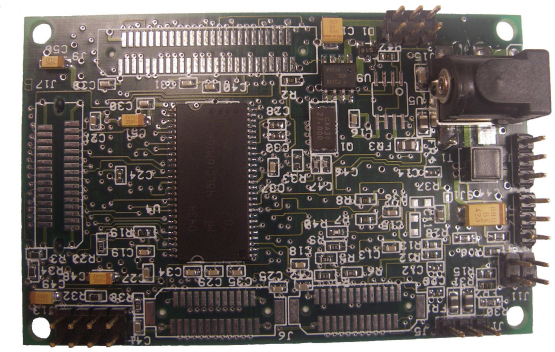
# 1.0 Introduction





Bottom

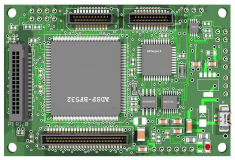
**Features:**

- Blackfin ADSP-BF532 400MHz DSP Processor
- AVR ATmega642 8MHz Supervisor Processor
- 32Mbytes SDRAM
- 512Kbytes Flash (1,2M optional)
- 2 RS-232 Ports, RS-485 Port
- 8Ch 10 bit A/D
- General Purpose Video Input Port
- 8 Bi-directional I/O ports
- Blackfin Memory/SPORT Expansion Port
- AVR Analog/Digital Expansion Port
- Blackfin JTAG/AVR ISP Programming Ports
- Extensive Source code examples
- GNU C compiler for both processors
- 5-7VDC input, 3.3V on board @10-250ma
- Small form factor (2.9x1.9in)

## Hardware – Blackfin/AVR

The P1 is a dual processor board with a 400MHz Blackfin processor and an 8MHz ATmega16 processor. The Blackfin is a high performance 16 bit RISC DSP with dual MACs, multiple accumulators with 84Kbytes of internal program and data cache. The Blackfin is capable of 600MMACs and is designed for ultra fast image processing and general purpose processing. Programs are loaded from a 512Kx8 Serial Flash and execute from a 16Mx16 133MHz SDRAM. The SDRAM provides both program and data storage. The video expansion port accepts several color and BW camera modules or can be used as a high speed general-purpose data port. A memory expansion bus supports additional peripheral daughter boards. The Blackfin ultra high-speed serial ports (SPORTS) are available on another expansion port. A Blackfin JTAG emulation port and RS-232 serial port allows local communication. A real time clock provides self timed sleep capability with several power down modes. The Blackfin communicates with the AVR using an SPI port.

The AVR processor is an 8MHz self clocked general purpose controller with 8 10bit A/D channels, 8 general purpose bi-directional digital IO channels, a RS-232 port, RS-485 port and 2-Wire port. The AVR processor has 64Kbytes of Flash, 4Kbytes SRAM and 2Kbytes EEPROM. The 2-Wire (TWI) port is a general purpose 2-wire party line communications bus that connects multiple AVR satellite processors with remote wake-up, node ID identification and high-speed data transfer (>400Kbits/sec). The AVR communicates with the Blackfin and 1Mx8 Serial Flash via a high speed SPI port. The AVR controls the Blackfin reset line and can provide initial boot code to the Blackfin after reset is released. Alternatively the Blackfin can boot from Flash (Boot Mode 3). A real time clock allows the AVR to enter a deep sleep low power state with clock or external event (TWI) wake-up.



Several daughter cards are available for interface expansion flexibility – video, LCD displays, TWI modules, Ethernet and FPGA. Small form factor connectors bring out Blackfin memory, SPORT and video lines while the AVR expansion connector adds SPI, analog/digital and TWI lines.

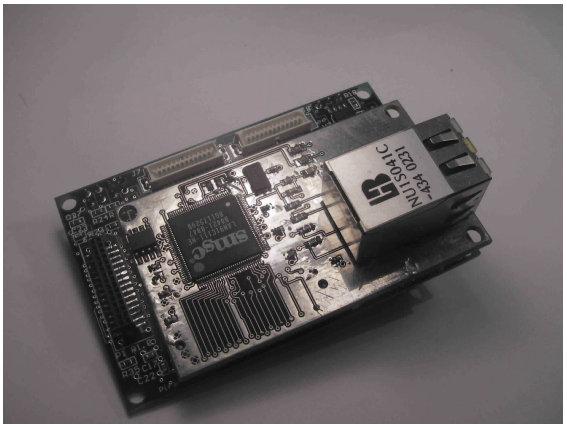


Figure 1-1. P1 with APS12 Ethernet daughter card.

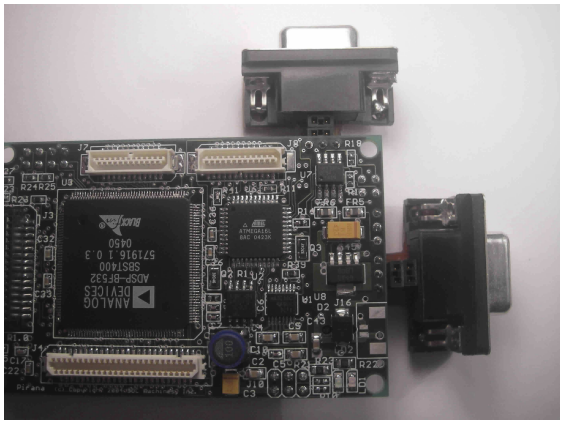
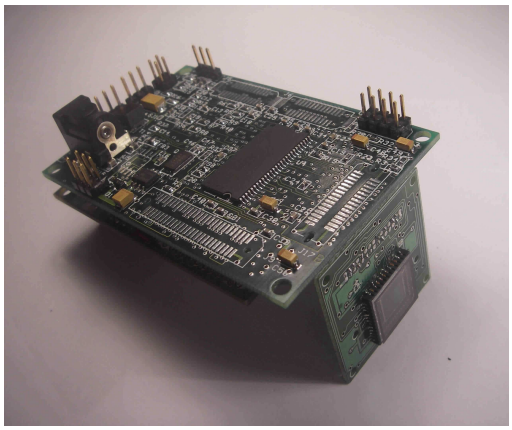


Figure 1-2. P1 with serial adapters attached.

P1 daughter cards greatly extend the interface options of the basic P1. The picture below shows the APS12 10/100 Ethernet and CM200-20 2Mpixel CMOS imaging module mounted on a P1. Note that daughter cards can be mounted vertically or horizontally.



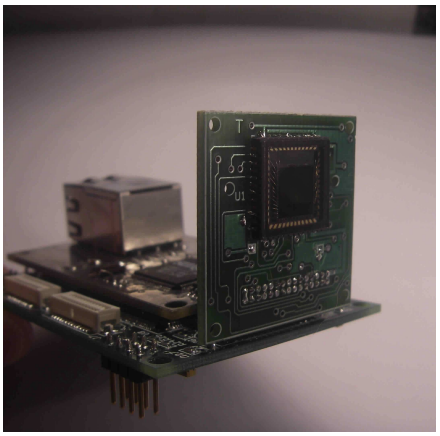


Figure 1-3. P1 with APS12 Ethernet and CM200-20 daughter cards attached.

# 2.0 Quick Start Guide

For PCB Revision 1.0b

Thank you for purchasing the P1 Development Kit V1.13b. Before you begin to use the P1 read the following startup procedure and cautions.

The P1 is a dual processor embedded DSP for video processing. The P1 has two processors - Blackfin and AVR - each with it's own serial channel and boot monitor. The P1 comes pre-loaded with a boot monitor for each processor. Included is the complete source code for both boot monitors. The Blackfin Boot Monitor supports the download of Intel Hex files created by the Analog Devices elfloader.exe utility. The AVR is programmed via the included 6-pin ISP cable. The P1 has a non-standard Blackfin JTAG port (adapter required to mate with the standard Analog Devices JTAG cable – there wasn't room for a full size connector). The Blackfin processor is an ADSP-BF532 Rev 0.3 silicon part that boots from Atmel SPI Flash devices – the P1 comes with one 1Mx8 Flash device installed.

The P1 Boot Monitors are continuously upgraded – check the SOC Robotics, Inc web site for new software updates.

**WARNING:**

1. **Do not attach or detach the programming cable while the unit is powered – always remove power from the unit first. Remove the programming cable before shutting the PC off or rebooting the PC – leaving the cable attached may result in erasure of the AVR Flash memory.**
2. **The P1 requires regulated DC between 4.2 to 6VDC – do not exceed this range – damage to the onboard LDO regulator may result. Many low cost wall mount DC power adapters exceed their rated output under light load.**
3. **The Blackfin and AVR processors share common signals. Carefully review the schematics and documentation before changing any of these signals in software.**

## Revision 0.72/0.92 Boot Monitor

The CD includes complete source code for the AVR and Blackfin Boot Monitors. The AVR Boot Monitor was developed using ImageCraft ICCAVR Version 7.13. ImageCraft ICCAVR is available as a time limited free trail from the ImageCraft web site. The Blackfin Boot Monitor was developed using Analog Devices VisualDSP++ V4.5. VisualDSP is available from Analog Devices as a time limited free trial. Project files are included for both processors – this should save time for new application development.

## Hardware Setup

The Blackfin serial port (J2) is set to 115,200baud, 8 data bits, one stop bit and no parity with XON/XOFF flow control disabled. The AVR serial port (J1) is set to 38,400baud, 8 data bits, one stop bit, no parity and no flow control.

1. Remove the P1 from the anti-static bag and place on a non-conducting surface. The P1 is pre-loaded with a boot monitor for each processor. For the moment leave the ISP-6 programming adapter unattached. Connect a DC power source between 5-6VDC - the P1 has a reverse polarity protection diode. The power supply must not exceed 6.5VDC or damage to the LDO regulator may occur – the power plug is center pin positive.
2. The P1 requires two custom serial cables (not supplied). The AVR serial port connector (J2) is located next to the DC power jack. The Blackfin serial port connector is located next to the 25pin AVR I/O port connector.

3. Start Hyperterminal (or equivalent program), set the baud rate 38,400 for the AVR and 115,200 with XON/XOFF flow disabled for the Blackfin.
4. Plug in DC power. The unit should power-up with the RED and GREEN LEDs flashing twice then the GREEN Led flashing continuously. Both processors output a sign-on message on each serial channel and then wait for commands.
5. The AVR boots from internal Flash. The AVR sets the Blackfin Boot Mode to 3 (see Analog Devices Engineer-to-Engineer Note 240) and resets the processor. The P1 boots from external SPI Serial Flash.
6. The P1 Boot Monitor includes functions for set/change memory, downloading and uploading IntelHex32 files and exercising various daughter cards.
7. The AVR Boot Monitor provides similar functions.

## Software Setup

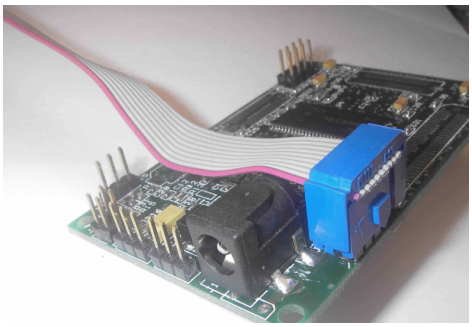
P1 Software Development tools are available from several sources. Open source GNU C compilers are available for both processors from www.blackfin.org. An open source GNU debugger GDB is available to debug GNU applications via a parallel port JTAG adapter. Professional software development tools are available from ImageCraft and Analog Devices (both firms offer free trial periods). The Blackfin and AVR Boot Monitors were developed using VisualDSP++ 4.5 and ICCAVR 7.13 respectively – project files for both environments are included on the CD.

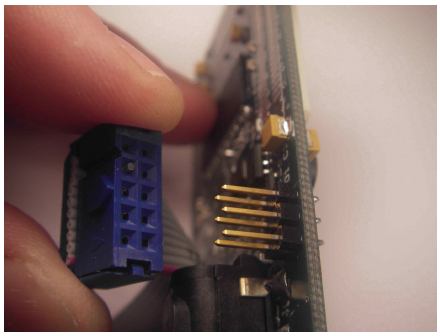
## Programming P1 Flash

AVR Flash is reprogrammed using the ISP10 programming adapter. Blackfin external SPI Flash is reprogrammed in two steps. Hex files for the AVR and Blackfin Boot Monitors is included on the CD (AVR – P1_Monitor.hex, Blackfin - P1_ldr.hex).

### AVR Flash Programming

To reprogram the AVR Flash remove power from the P1, attach the ISP10 Programming Adapter (as shown in the picture – the connector is keyed) to the ISP connector (J10 – below DC Power Jack) and apply power.





Using PonyProg2000 (or a similar Windows/Linux programming tool) download the new program to the AVR Flash. Note that the AVR controls the Blackfin boot process – this process must be preserved in all new AVR programs if the Blackfin is to boot properly.

### Blackfin Flash Programming

Programming Blackfin Serial Flash is a two step process - download a new program to SDRAM via the Blackfin serial port then move the program image to Serial Flash using the "M" (MOVE) command. The

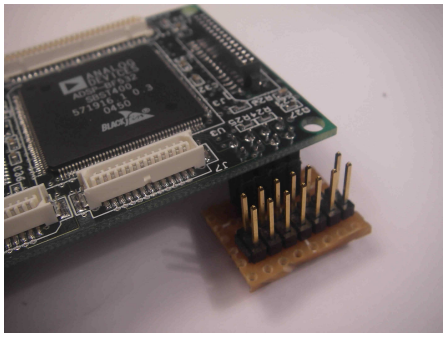
Blackfin Boot Monitor interprets both IntelHex16 and IntelHex32 files directly. There is a bug in the direct IntelHex to SPI Flash function so do not use this function.

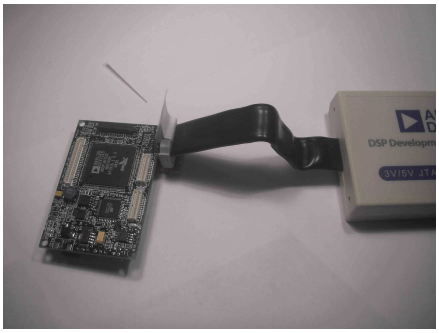
### Programming Caution

The AVR and Blackfin processors are both connected to the two Atmel SPI Serial Flash devices using shared MOSI/MISO/SCK lines. To access Serial Flash either the Blackfin or AVR acts as a SPI Master – the other processor must release the SPI lines at this time. During a Mode 3 boot the Blackfin becomes SPI Master and attempts to boot from the SPI Flash. The current version of the Blackfin Boot Monitor leaves the Blackfin as SPI Master following the boot. For the AVR to access the SPI Flash it must reset the Blackfin then allow the Blackfin to attempt to boot under Mode 0 (parallel flash boot) – this frees the SPI lines for access by the AVR while leaving the Blackfin in an unknown state. The reset line is connected to the SPI Flash chip to ensure the Flash is reset to a known state. In a future release of the Boot Monitors a protocol will resolve access to the SPI Flash during run time – for the moment the Blackfin must be reset and rebooted using Boot Mode 0 – once the AVR is finished with the SPI Flash it restarts the Blackfin using Boot Mode 3.

### Blackfin JTAG Port

The Blackfin 8 pin JTAG port can be converted the Analog Devices 14 pin emulator compatibility using an optional adapter board.





## Boot Monitor Known Bugs

The following know bugs will be fixed in the next release. Check the SOC Robotics web site for new updates.

The Blackfin direct serial port to Flash Intel Hex load command does not work – use the two step load process.

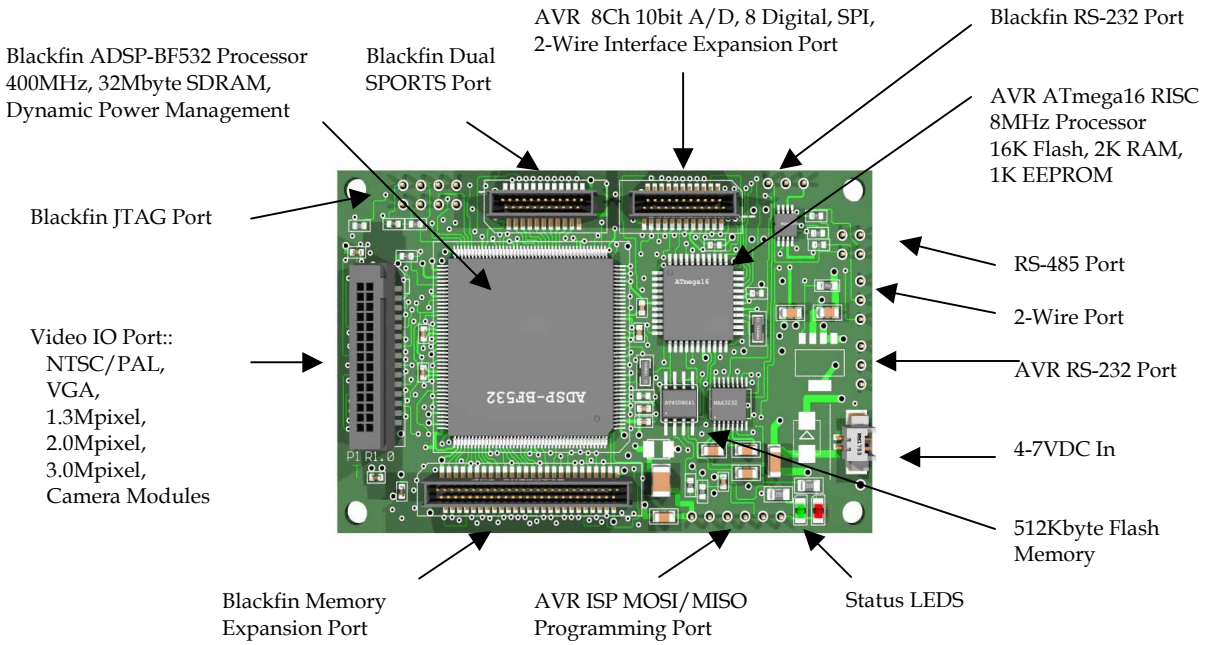
## Next Release Features

In the next release of the AVR Boot Monitor SPI Flash read/write support will be implemented. This command will allow the AVR to reprogram Blackfin Serial Flash thereby allowing the Blackfin Boot Monitor to be reloaded if accidentally erased.

# 3.0 Detailed Description

## 3.1 Introduction

The P1 is a dual processor high performance embedded video processing and general-purpose controller engine. About the size of a business card the P1 has a 400MHz Blackfin DSP processor with Dynamic Power Management and an 8MHz self clocked AVR Atmega642 Flash processor for general IO and Blackfin management. Blackfin memory consists of 16Mx16 133MHz SDRAM and 1Mx8 Flash. The Flash can be increased to 8Mx8. The AVR processor has 64K bytes of internal Flash, 4K of internal SRAM and 2K of internal EEPROM. Dynamic power management allows both processors to enter a deep sleep state dropping power to the low mA range. Dual real time clocks provide continuous current time tracking. A general-purpose video port supports a variety of camera modules from NTSC to 3Mpixel. The AVR has 8 10bit A/D channels, 8 digital IO lines a TWI port, RS-232 port and RS-485 port. The 2-Wire serial bus provides seamless attachment of additional AVR data acquisition processors.



## 3.2 Blackfin Processor

The P1 Blackfin processor (ADSP-BF532) is a 400MHz DSP processor core with dual MACs, serial port, SPI port, video expansion port, dual SPORTS, memory expansion and core voltage regulator. The Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file and is capable of 800 million MAC operations per second. See the ADSP-BF532 specification sheet for detailed processor information. The P1 uses Revision 0.3 silicon. See the ADSP-BF532 errata for specific chip operation quirks.

**Blackfin Features:**

Up to 400MHz high performance Blackfin processor
Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs,
40-bit shifter
RISC-like register and instruction model for ease of programming and compiler-friendly support
Advanced debug, trace, and performance monitoring
0.8 V to 1.2 V core VDD with on-chip voltage regulation
3.3 V and 2.5 V tolerant I/O

**MEMORY**

Up to 148K bytes of on-chip memory:
- 16K bytes of instruction SRAM/Cache
- 32K bytes of instruction SRAM
- 32K bytes of data SRAM/Cache
- 4K bytes of scratchpad SRAM

Two dual-channel memory DMA controllers
Memory management unit providing memory protection
External memory controller with glueless support for SDRAM, SRAM, FLASH, and ROM
Flexible memory booting options from SPI and external memory

**PERIPHERALS**

Parallel peripheral interface (PPI)/GPIO, supporting
ITU-R 656 video data formats
Two dual-channel, full duplex synchronous serial ports, supporting eight stereo I2S channels
12-channel DMA controller
SPI-compatible port
Three timer/counters with PWM support
UART with support for IrDA®
Event handler
Real-time clock
Watchdog timer
Debug/JTAG interface
On-chip PLL capable of 1× to 63× frequency multiplication
Core timer

The P1 Blackfin has 32Mbytes of 133Mhz SDRAM organized as 16Mx16. The SDRAM starts at address 0x00000000 and goes to 0x1fffffff. A 27.000MHz external crystal is multiplied then divided to generate the 400MHz internal core clock (CCLK) and 130MHz system clock (SCLK). Two Serial Flash devices connected to the Blackfin SPI port provide 512Kx8 to 8Mx8 boot memory each. The Blackfin code executes from on chip instruction and data cache and from SDRAM. The programmer allocates code and data to on chip cache and off chip SDRAM at link time.

### System Clock

The Blackfin is clocked by an external 27Mhz crystal that is multiplied and divided by the internal PLL to generate a 398MHz core clock (CCLK) and 130MHz system clock (SCLK). The Blackfin Boot Monitor sets the multiplier and divider values. SCLK is the master clock for on chip peripherals.

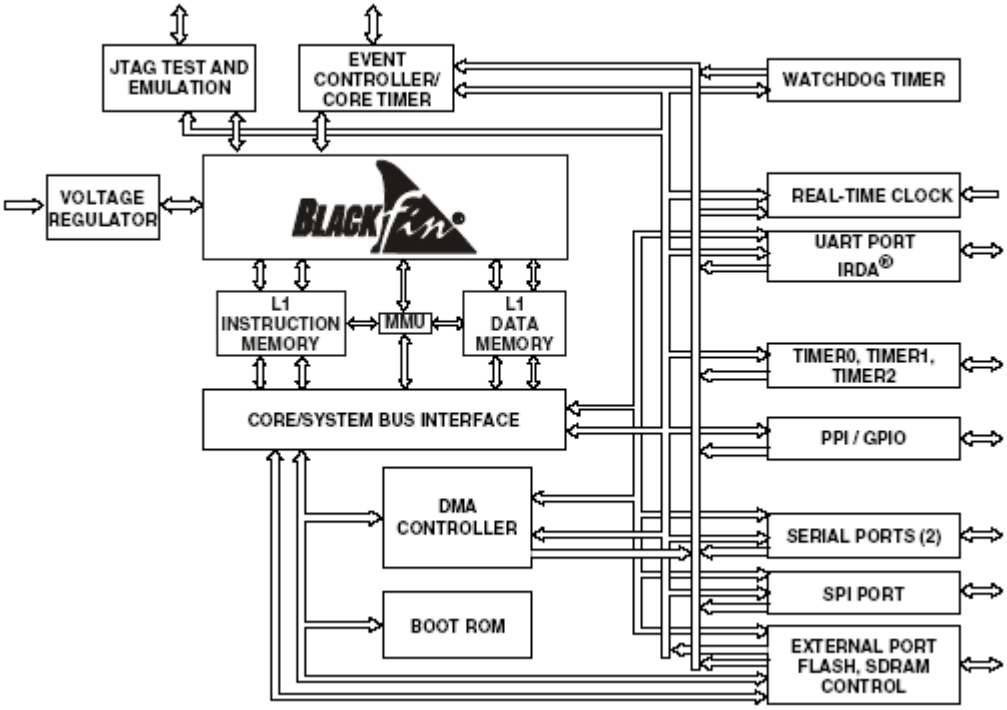



Figure 3-4. Blackfin functional diagram.

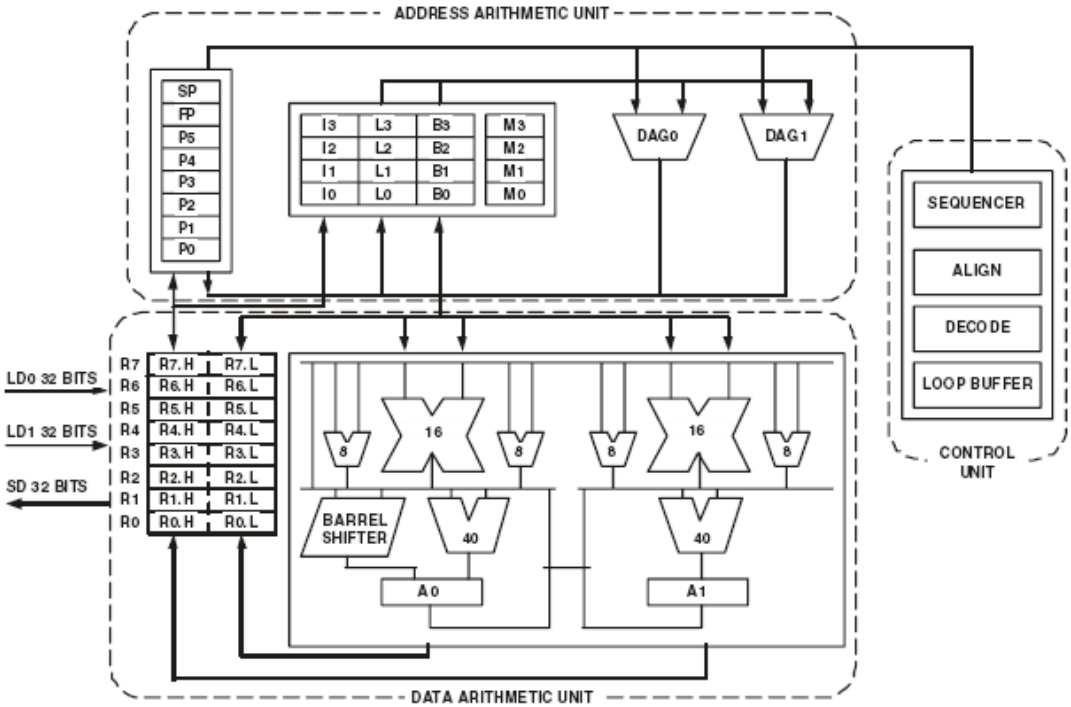


Figure 3-5. Blackfin ALU structure.

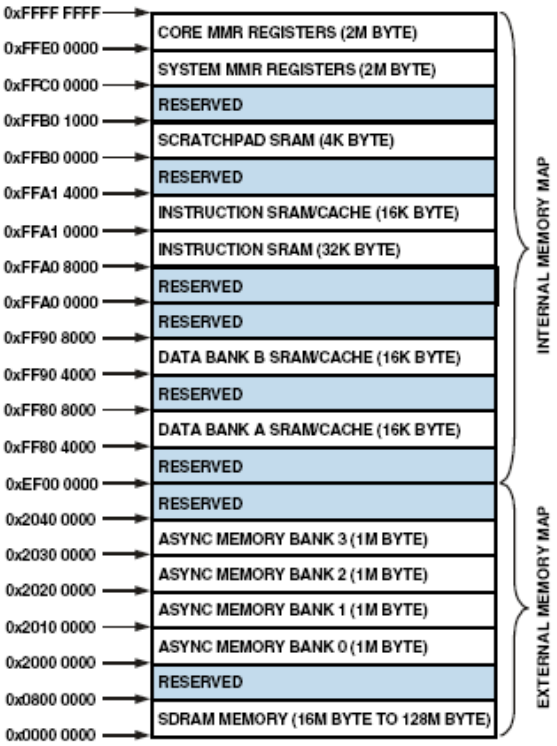



Figure 3-6. Blackfin processor memory map.

## Memory Map

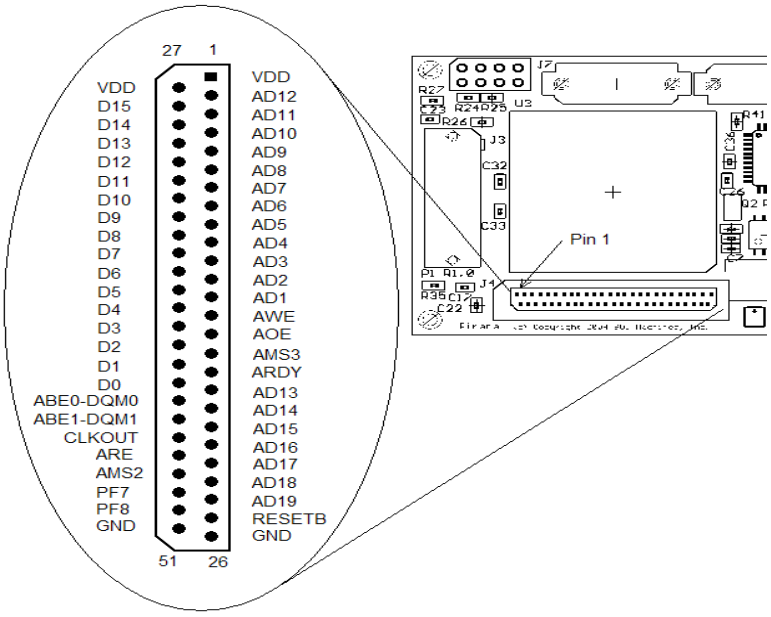
The Blackfin memory map is shown in the diagram above. The 32Mbyte SDRAM starts at address 0x00000000 and ends at 0x1FFFFFF. SDRAM timing is set by writing parameters to SDRAM setup registers. The Blackfin Boot Monitor sets up the SDRAM control registers. Asynchronous memory chip selects AMS2 and AMS3 are routed to memory expansion connector J4/J9 and AMS0 and AMS1 are routed to SPORT connector J6/J7. Asynchronous memory chip select timing (setup times, wait states, etc) is individually programmable for each chip select.

## Expansion Options – Memory, Video, SPORT

The Blackfin processor expansion options consist of a memory expansion port (signal lines routed to connector J4/J9), video expansion port (signal lines routed to J3/17) and SPORT expansion port (signal lines routed to J6/J7). Blackfin external memory architecture supports multi-master operation via the BG, BR and BGH signal lines.

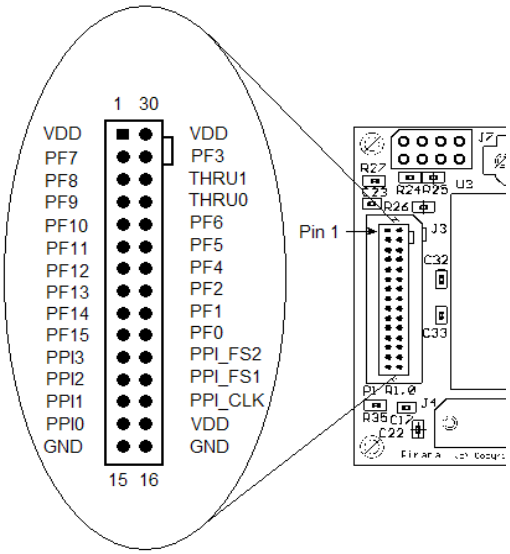
## Memory Expansion Port

The Blackfin memory expansion port supports most of the Blackfin memory signal lines on connector J3 (top) and J17 (bottom). Two video expansion port signal lines (PF7, PF8) can be used as interrupts. Asynchronous chips selects AMS2 and AMS3 provide simple daughter card selection.



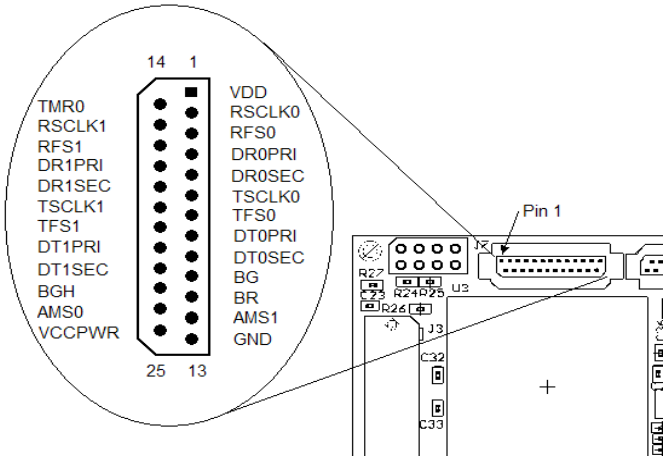

## Video Expansion Port

The P1 Blackfin video expansion port is routed to connector J4 (top) and J9 (bottom). The top connector is a SAMTEC SFM15 that mates to a SAMTEC right angle or horizontal connector allowing video daughter cards to be mounted vertically or horizontally. The bottom connector is a Hirose DF9-31P. The Blackfin video port directly supports ITU-R 656 video streams but can also be used as a general purpose high speed bi-directional data port. PF2 and PF3 select Serial Flash U2 and U5 respectively. Maximum port speed is related to SCLK – maximum speed is 66MHz. The Blackfin Boot Monitor sets the Video port registers for high speed video transfer with DMA support.



## SPORT Expansion Port

The Blackfin has two high speed SPORT channels routed to connector J6 (top) and J7 (bottom). Processor Bus request/grant arbitration lines (BR, BG and BGH) are routed to this connector enabling the development of multi-processor daughter cards. Asynchronous chip selects AMS0 and AMS1 are routed to this connector. To support high power levels Unregulated DC (VCCPWR) is also routed to this connector so daughter cards can generate their own VDD (3.3V).




## Serial Flash

Two Serial Flash devices (U2, U5) provide up to 16Mx8 of program/data storage. The Serial Flash is accessed using the SPI lines. The Blackfin and AVR access Serial Flash as SPI Masters. U2 is selected by PF2 and U5 by PF3. PF2 and PF3 are connected to AVR pins PB4/PC5 and PD2 respectively. Supported Serial Flash devices are Atmel AT45DB041 (512x8), AT45DB081 (1Mx8) and AT45DB161 (2Mx8), AT45DB321C (4Mx8) and AT45DB642D (8Mx8). Note that the Blackfin processor internal boot code supports the first three devices but not the last two. The Blackfin Boot Monitor has code examples for reading and writing Serial Flash.

## Internal Peripherals – USART, SPI, I2C, Real Time Clock

### USART

The on chip USART is connected to an RS-232 transceiver and routed to connector J1. Registers set baud rate, bits, parity, etc. An interrupt driven serial driver is included in the Blackfin Boot Monitor with full XON/XOFF flow control.

### SPI

The on chip SPI peripheral (MOSI, MISO, SCK and slave chip selects) is used to communicate with the Serial Flash devices, AVR and external devices via the AVR expansion port. The Blackfin supports SPI Master or Slave operation. The Blackfin accesses Serial Flash device U2 under a boot Mode 3 restart via the SPI lines - one video port pin PF2 is used as a Flash chip select.

### I2C

Two lines of the video expansion port are used to implement an I2C function. I2C is a two line communications protocol for peripheral management using SDA and SCL. The Blackfin does not have a

hardware I2C peripheral so the Boot Monitor implements a software I2C controller. The specific pins allocated to SDA and SCL is user settable. A description of I2C protocol is included with the kit CD.

### Real time clock

An external 32.768KHz crystal provides a real time clock. The Blackfin real time clock is designed to provide time of day and other control functions for system startup from sleep conditions.

## 3.3 AVR Processor

The AVR is an Atmel Atmega642 8bit 8MHz RISC processor with a multitude of on- chip peripherals and IO options. The AVR is the peripheral IO engine for the Blackfin processor. The AVR and Blackfin share a number of common signals and communicate over a high speed (2Mbps) SPI bus. The Atmega16 is programmed in C using GNU or Commercial 3rd party tools.

AVR key features:

- **High-performance, Low-power AVR® 8-bit Microcontroller**
- **Advanced RISC Architecture**
  - **131 Powerful Instructions – Most Single-clock Cycle Execution**
  - **32 x 8 General Purpose Working Registers**
  - **Fully Static Operation**
  - **Up to 20 MIPS Throughput at 20 MHz**
- **High Endurance Non-volatile Memory segments**
  - **64K Bytes of In-System Self-programmable Flash program memory**
  - **2K Bytes EEPROM**
  - **4K Bytes Internal SRAM**
  - **Write/Erase cyles: 10,000 Flash/100,000 EEPROM(1)(3)**
  - **Data retention: 20 years at 85℃/100 years at 25° C(2)(3)**
  - **Optional Boot Code Section with Independent Lock Bits**

**In-System Programming by On-chip Boot Program**
**True Read-While-Write Operation**

  - **Programming Lock for Software Security**
- **JTAG (IEEE std. 1149.1 Compliant) Interface**
  - **Boundary-scan Capabilities According to the JTAG Standard**
  - **Extensive On-chip Debug Support**
  - **Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface**
- **Peripheral Features**
  - **Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes**
  - **One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode**
  - **Real Time Counter with Separate Oscillator**
  - **Six PWM Channels**
  - **8-channel, 10-bit ADC**

**Differential mode with selectable gain at 1x, 10x or 200x**

  - **Byte-oriented Two-wire Serial Interface**
  - **One Programmable Serial USART**
  - **Master/Slave SPI Serial Interface**
  - **Programmable Watchdog Timer with Separate On-chip Oscillator**
  - **On-chip Analog Comparator**
  - **Interrupt and Wake-up on Pin Change**
- **Special Microcontroller Features**
  - **Power-on Reset and Programmable Brown-out Detection**
  - **Internal Calibrated RC Oscillator**
  - **External and Internal Interrupt Sources**
  - **Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby**
- **I/O and Packages**
  - **32 Programmable I/O Lines**
  - **40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF**
- **Speed Grades**
  - **ATmega644V: 0 - 4MHz @ 1.8 - 5.5V, 0 - 10MHz @ 2.7 - 5.5V**
  - **ATmega644: 0 - 10MHz @ 2.7 - 5.5V, 0 - 20MHz @ 4.5 - 5.5V**
- **Power Consumption at 1 MHz, 3V, 25°C**
  - **Active: 240 µA @ 1.8V, 1MHz**
  - **Power-down Mode: 0.1 µA @ 1.8V**

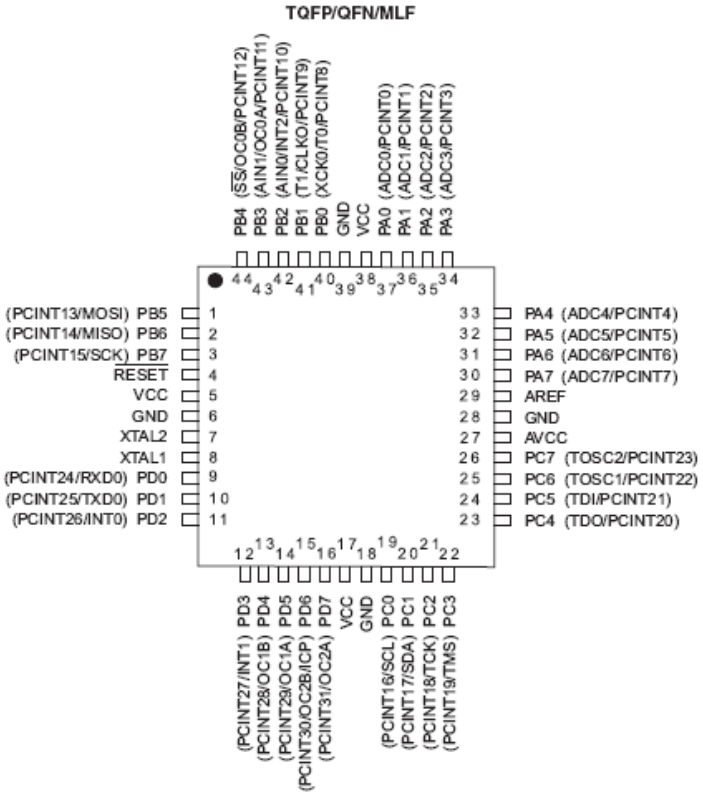



Figure 3-3. AVR Atmega642 chip pin assignment.

The Atmega642 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the Atmega642 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed. The AVR has 64Kbytes of internal Flash, 4Kbytes of internal SRAM and 1Kbytes of EEPROM. The AVR Flash is programmed using an ISP6 Programming Adapter. The ISP6 connects to a PC's parallel port and loads programs via the SPI pins (MOSI, MISO, SCK, RESET). The AVR controls the boot mode of the Blackfin.

## Real Time Clock

A 32.768KHz crystal is connected to real time clock inputs PC6, PC7 providing a real time clock option for timed data acquisition applications and calibration of the internal 8Mhz clock. The Atmega642 generates the master system clock using an internal oscillator (no external crystal) which may be uncalibrated. This oscillator can be calibrated by using the real time clock to accurately time a one second delay which is then used to adjust the master clock oscillator. The AVR Boot Monitor includes a sample real time clock example.

## ADC Subsystem

The Atmega642 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer that allows 8 single-ended voltage inputs on pins PA0 to PA7. Pins PA0 to PA7 are brought out to connectors J5/J8. Maximum sample rate is 15Ksps at the maximum resolution. The single-ended voltage inputs refer to 0V (GND). The device also supports 16 differential voltage input combinations. Two of the differential inputs (ADC1, ADC0 and ADC3, ADC2) are equipped with a programmable gain stage, providing amplification steps of 0 dB (1x), 20 dB (10x), or 46 dB (200x) on the differential input voltage before the A/D conversion. Seven differential analog input channels share a

common negative terminal (ADC1), while any other ADC input can be selected as the positive input terminal. If 1x or 10x gain is used, 8-bit resolution can be expected. If 200x gain is used, 7-bit resolution can be expected. The ADC contains a Sample and Hold circuit that ensures the input voltage to the ADC is held at a constant level during conversion. The ADC has a separate analog supply voltage pin, AVCC that is filtered by R14/C11 from the 3.3VDC. Internal reference voltages of nominally 2.56V or AVCC are provided On-chip. The voltage reference may be externally decoupled at the AREF pin by a capacitor for improved noise performance. The Programmer selects either 2.56V or 3.3V for AREF. The AVR Boot Monitor includes an example multiplexed A/D routine.

### Serial Peripheral Interface - SPI

The Atmega642 Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the Atmega642 and the Blackfin processor or between other SPI devices via AVR expansion port J5/J8. The SPI is a full-duplex, three-wire (MOSI, MISO, SCK) Synchronous Data Transfer communication port with Master or Slave operation, LSB first or MSB first data transfer, seven programmable bit rates, End of Transmission interrupt flag, Write Collision flag protection, wake-up from Idle Mode and double speed (CK/2) Master SPI Mode. Maximum SPI clock rate is 2Mhz. The Atmega642 can read or write the two Serial Flash devices under program control. SPI provides high speed full duplex communication between the AVR and Blackfin processor. The AVR Boot Monitor includes code to read and write the Serial Flash devices.

The Atmega642, Blackfin and two Serial Flash devices (U2, U5) have their SPI lines connected together. To access the Serial Flash devices either the Blackfin or the Atmega642 must operate as a Master SPI controller and activate the appropriate Flash chip select. Only one processor is able to operate as a Master – the other must act as Slave or be disabled. The table below shows which lines are common to the Blackfin and Atmega642. The Programmer has control of these lines and can also use them to gain the attention of the other processor.

Table 3.3. Blackfin/AVR SPI Serial Flash common signal lines.

| Blackfin | ATmega16 | Flash CS |
|---|---|---|
| PF0 | PB4,PC5 | U2 |
| PF3 | PD2 | U5 |

### TWI Interface – I2C

The Two-wire Serial Interface (TWI) provides the P1 (via the AVR) with an I2C communications capability for off board peripheral communication via connector J12. The TWI protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The TWI lines are pulled high so the default state is idle. All devices connected to the TWI bus have individual addresses and mechanisms for resolving bus contention are inherent in the TWI protocol. Both Master and Slave operation is supported along with multi-master arbitration support, up to 400 kHz data transfer speed, slew-rate limited output drivers with ferrite bead EMI snubbers on each line, fully programmable slave address with general call support and address recognition causes wake-up when AVR is in sleep mode. The Blackfin Boot Monitor includes code that setup the TWI interface as a Master.

Several TWI modules including audio, compass, accelerometers, color LCD, DC motor control, stepper motor control and general analog/digital IO are available from SOC Robotics to enhance and extend the IO functions already available on the P1. See the SOC Robotics web site for more information.

## General Purpose I/O

The AVR Expansion port brings AVR functions SPI, TWI, ADC PA0-7, AREF, AVCC, PB0-4, PD2 and PD7 to connectors J5/J8. Analog input pins PA0-7 can also operate as digital I/O ports on an individual pin basis. Digital port pins PB0 to PB4 are pulled high with 10K resistors. VCCPWR is the unregulated DC input. VDD is 3.3V and AREF is the filtered analog voltage reference. TWI lines SDA and SCL are pulled high. SPI lines MOSI, MISO and SCK coupled with PB0-4, PD2 or PD7 provide up to 7 SPI slave chip selects. PB4 is the Atmega642 slave SS\ select pin and is also attached to PF0 via a 1K resistor.

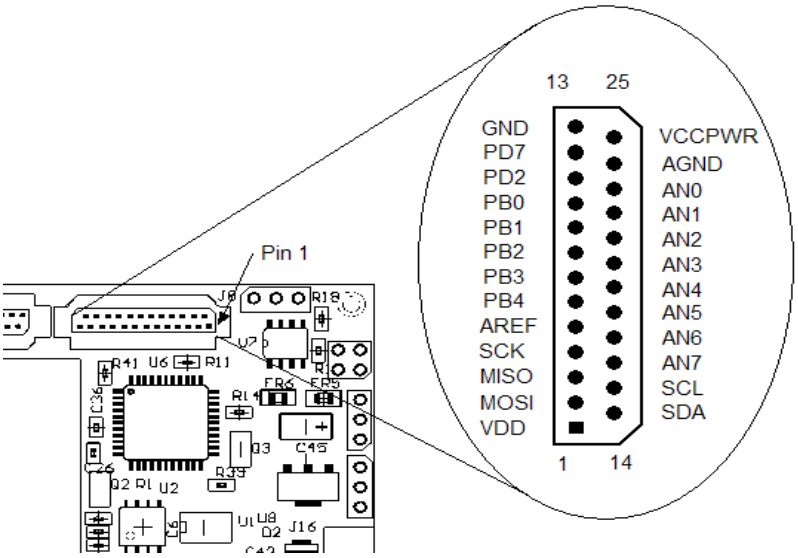



Figure 3.5. AVR expansion port connectors J5/J8.

## RS-232 Serial Port

The Atmega642 USART TX (PD1) and RX (PD0) lines are connected to RS-232 transceiver chip U1 and then to connector J1. The full duplex USART supports various baud rates, stop bit and parity. USART operation is interrupt driven with multiple interrupt sources. The AVR Boot Monitor includes a full interrupt driven USART driver.

## RS-485 Serial Port

The Atmega642 supports an RS-485 serial port using pins PC3 (TX) and PC2 (RX). Full duplex RS-485 serial transmit and receiver operation is software based as no serial hardware is available for this function in the Atmega642. The software implementation limits the maximum speed of the RS-485 line to about 9,600 baud. As the serial protocol engine is software based different signaling protocols such as synchronous or asynchronous can be implemented. The software UART is driven by a clock interrupt.

## Serial Flash

The P1 has pads for two Serial Flash devices ranging in size from 512Kx8 to 8Mx8 each. The standard P1 ships with a 1Mx8 Flash – the user can install a second Serial Flash. The AVR communicates with the Serial Flash using the SPI communication bus. Pins PB4/PC5 select U2 – the first Serial Flash and PD2 selects U5 – the second Serial Flash. Note that PB4 and PC5 are connected together via a 1K resistor. This configuration allows the Blackfin (Master) to communicate with the AVR (Slave) by using the SS\ slave select pin. The AVR Boot Monitor contains a complete Serial Flash reader/writer.

### Blackfin Boot and Reset

The AVR controls the boot mode of the Blackfin processor by setting Blackfin mode pins BMODE1 (PD5) and BMODE0 (PD4). The Blackfin can boot from an external ASYNC0 memory (Mode 0), parallel 8/16bit flash (Mode 1), SPI Master with Blackfin as SPI Slave (Mode 2) or SPI Serial Flash (Mode 3). The P1 supports Boot Modes 2 and 3. Typical boot operation is for the AVR to reset the Blackfin, select the appropriate boot mode (default is Mode 3 – boot from Serial Flash) then release reset. If the AVR selects boot Mode 2 then the Blackfin retrieves boot information from AVR Flash rather than Serial Flash. The Blackfin Boot Monitor code (which loads from Serial Flash in Mode 3) sets up the SDRAM, core clock and system clock – the Boot Loader transfers code from Serial Flash to Blackfin Cache and external SDRAM based in the memory map of the application. By using Mode 2 it becomes possible for the AVR to direct the Blackfin ROM boot code to load the appropriate application program based on external events such as analog and/or digital data value or TWI state. For a better understanding of the Blackfin boot process see Application Note EE-240.

The AVR directly controls the Blackfin Reset line (PD3). The Reset line also resets the Serial Flash devices. By activating the reset line (active low) the Blackfin is forced to reload it's program from either Serial Flash or AVR Flash. Any AVR applications must manage the Boot Mode pins and reset line carefully to ensure reliable Blackfin operation.

## 3.4 Shared Lines

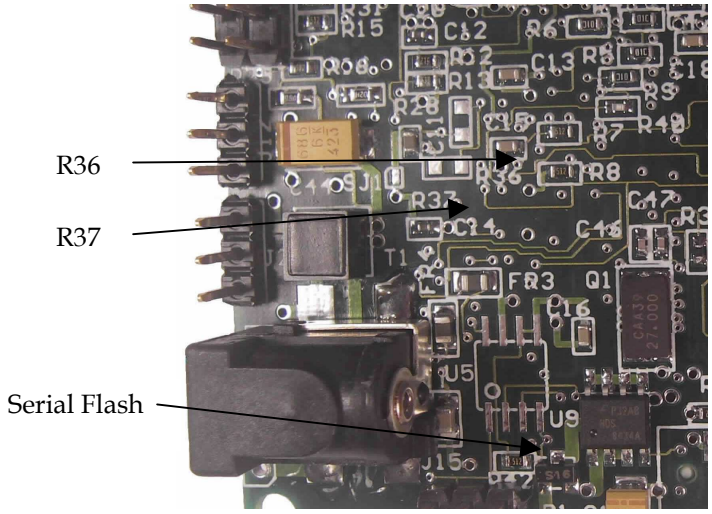
The Blackfin and AVR share several common signal lines. The following three Blackfin video port lines are connected to AVR signal lines: (PF0 – PB4/PC5), (PF2 – PC4) and (PF3 – PD2). A 1K resistor connects PF0 to PB4 and PF2 to PD2 to limit current in case both pins are accidentally driven at the same time. In addition both processor SPI signal lines (MOSI, MISO, SCK) are connected together.

To allow the Blackfin and AVR to access the Serial Flash devices both processor's SPI lines are connected to the Serial Flash devices.

## 3.5 Optional Parts

The P1 has two optional component configurations – temperature sensor (R36,R37) and a second serial flash (U7).

The temperature sensing circuit is a simple resistive divider. R36 and R37 are connected in series between VDD (3.3V) and GND. Values for R36 and R37 are selected by the user. R36 and R37 are located on the bottom of the board (see the picture below). By default these components are not installed.



The second Serial Flash (U5) is located on the bottom of the P1. Compatible Serial Flash devices are AT45DB041 (512Kx8), AT45DB081 (1Mx8), AT45DB161 (2Mx8), AT45DB321 (4Mx8), AT45DB641 (8Mx8).

# 4.0 P1 Software Development Environment

## 4.1 Introduction

The P1 can be programmed in C using two open source GNU C compiler tools – one for the Blackfin and one for the AVR. Third party Vendor Assembler and C tools are also available from Analog Devices, Atmel and other independent software vendors. This section describes the GNU C tools, boot modes and example programs. Contacts are provided for third party development tools.

Two open source operating systems are available fro the P1 – uCLinux and Ethernut OS. Both support an open source web server capability.

## 4.2 GNU C Tools

Two open source GNU C tool chains are available for the Blackfin and AVR C development. A current GNU C tool chain is provided for each processor with the P1 Hardware Development Kit. Professional C development tools are also available from third parties. If the GNU tool chain is used check to ensure you are using the latest release.

### 4.2.1 AVR GNU C Development Tools

The Atmega642 is programmed by loading a program into the internal 64K Flash. The AVR is programmed via ISP Port J10 using the ISP10 programming adapter and CISP.

The AVR GNU C tool chain is available for Windows and Linux platforms. The GNU C compiler must be configured to generate code for the Atmega642 processor. Once configured a number of sample programs including a Boot Monitor and Blackfin programming utility are provided to ease application development.

### 4.2.2 Blackfin GNU C Development Tools

The Blackfin is programmed by loading a program into the external Serial Flash memory chip. The external Flash can be programmed via the Blackfin serial line by downloading an Intel Hex16/32 file using the Blackfin Boot Monitor. Alternatively the AVR can program the external Serial Flash. The AVR controls the boot procedure of the Blackfin. The Blackfin has no internal Flash memory and must boot from an external source.

The GNU C tool chain is available for both Windows and Linux platforms.

## 4.3 System Boot Configurations

The P1 supports a number of boot options and configurations. The AVR boots from internal Flash while the Blackfin boots from either an SPI Master or External Flash. In a bare board configuration neither processor is able to boot. To facilitate application development the P1 Hardware Development Kit comes pre-programmed with a small boot kernel and Monitor already loaded into AVR and Blackfin Flash. AVR/Blackfin Boot Monitor source code is provided in.

The AVR boots from internal Flash and must be programmed before use. The boot kernel is pre-configured to boot the Blackfin from external Serial Flash (which is programmed with its own Boot Monitor program). The AVR Boot Monitor communicates with the host PC via the AVR serial port so the user can change Blackfin boot options. The AVR Monitor program is described in Section 4.4.

The Blackfin supports two boot configurations – Slave SPI and External Flash. In slave SPI mode a small boot kernel is loaded into the Blackfin from the AVR with the AVR acting as SPI Master. The Blackfin

then has the option to boot from Flash, the Blackfin serial port or via the AVR serial port and stored in AVR EEPROM. Typically the Blackfin executes from SDRAM so application programs must be loaded into SDRAM from Serial Flash prior to execution. The AVR Boot Monitor is described in Section 4.4.

## 4.4 Processor Boot Monitors

The P1 comes with a small boot kernel (Boot Monitor) pre-installed in each processor. The boot kernel uses the respective serial port to communicate with the host providing Hex16/32 file upload/download, Processor Reset, real time clock and peripheral initialization and test.

### 4.4.1 AVR Boot Monitor

The AVR Boot Monitor communicates with a host PC via the AVR serial port. Default serial communication settings are 9,600 baud, 8 data bits, 1 stop bit and no XON/XOFF flow control. The AVR Boot Monitor can change Flash and EEPROM contents, read the analog channels, run a test routine, change Blackfin boot mode and reset line and program the Serial Flash. The AVR is a sophisticated embedded controller. The ATmega16 datasheet is included in the CD.

### 4.4.2 Blackfin Boot Monitor

The Blackfin Boot Monitor communicates with a host PC via the Blackfin serial port. Default serial communication settings are 115,200 baud, 8 data bits, 1 stop bit and no parity. The Blackfin Boot Monitor contains an extensive set of initialization routines that setup all internal peripherals and communicate with the Serial Flash. The best way to become more familiar with Blackfin processor peripheral architecture is to review the Blackfin Boot Monitor source code along side the ADSP-BF532 Hardware Reference manual.

## 4.5 Open Source OS Support

Two open source operating systems are available for the P1 – uCLinux and Ethernut OS. uCLinux is a comprehensive Linux port for embedded processors while Ethernut OS is a lean event driven OS for embedded processors. Both support web server and TCP/IP applications.

### 4.5.1 uCLinux Support

An open source uCLinux port is available from www.blackfin.org. This port can be programmed into external Flash although at least 2Mx8 of Flash is required.

### 4.5.2 Ethernut OS Support – pNut

The Ethernut is a lean open source OS integrating a complete TCP/IP stack and web server for embedded applications. Ethernut OS was originally developed for the ATmega128 processor and has been ported to a number of embedded processors. The code base is now being ported to the P1 Blackfin and will be available as an open source OS web server platform. The Blackfin port is call pNut.

## 4.6 Example Programs

Several example programs are included for each processor to assist application development. Most of the programs are available as open source. A video processing library is included with drivers for five video interface modules. Check the SOC Robotics web site for the latest versions – www.soc-Robotics.com.

# 5.0 P1 Hardware Expansion Port Summary

## 5.1 Overview

The P1 has several IO expansion ports. The following table summaries the expansion connector ports on the P1. Note that different connector options are available to meet specific OEM requirements.

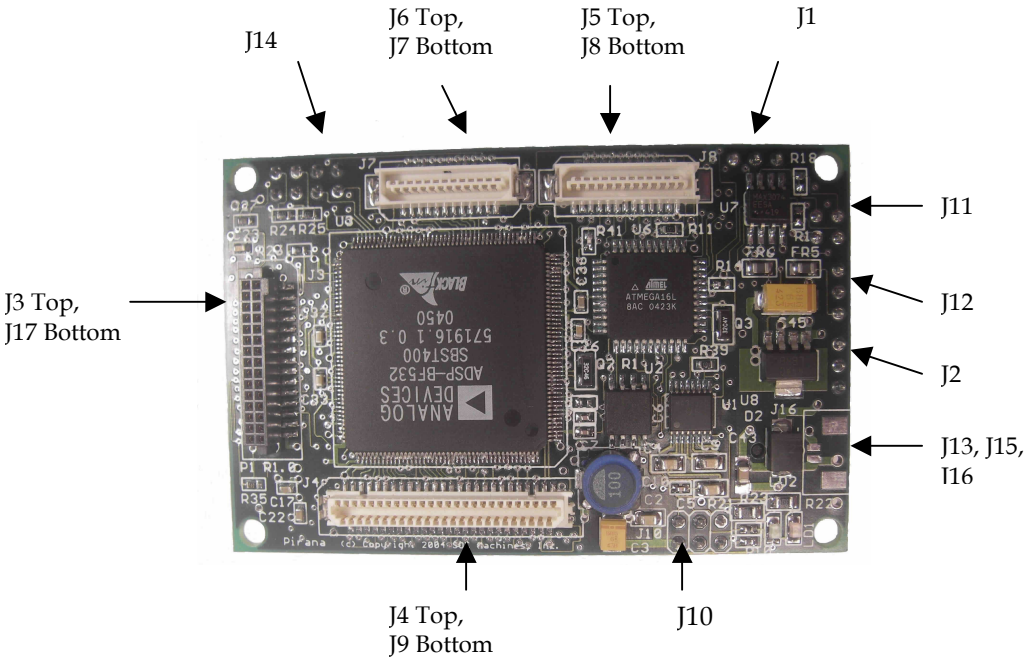



*Figure 5-1.* **P1 Connector locations**

| Connector | Description |
|---|---|
| J3/J17 | Video Expansion Port |
| J4/J9 | Blackfin Memory Expansion Port |
| J10 | AVR ISP Port |
| J13/J15/J16 | DC In Connectors |
| J2 | AVR RS-232 Serial Port |
| J12 | TWI Port |
| J11 | AVR RS-485 Port |
| J5/J8 | AVR Analog/Digital/SPI Expansion Port |
| J6/J7 | Blackfin SPORT Port |
| J14 | Blackfin JTAG Port |
| J1 | Blackfin RS-232 Serial Port |

## 5.2 Serial Ports – RS-232 and RS-485

The P1 has two RS-232 full duplex serial ports and one RS-485 full duplex serial port. The RS-232 serial ports run up to the full speed of the processor with a suitable interface chip. The RS-485 serial interface is available in three speed options – 115Kbps, 500Kbps and 10Mbps. The Blackfin Serial Port pins and AVR Serial Port pins are shown in Figure 5-2. The AVR RS-485 Serial Port pins in Figure 5-3.

***Figure 5-2.*** **J1 Blackfin Serial Port, J2 AVR Serial Port**

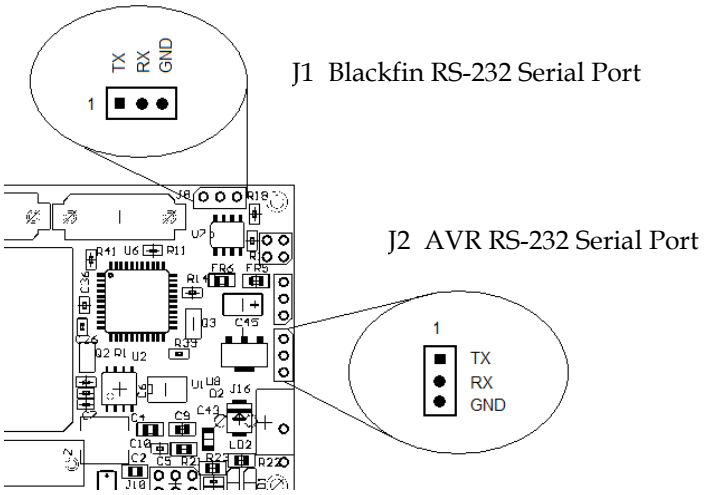
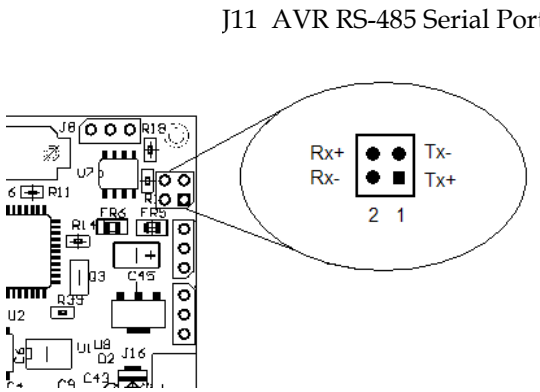



***Figure 5-3.*** **J11 AVR RS-485 Port**

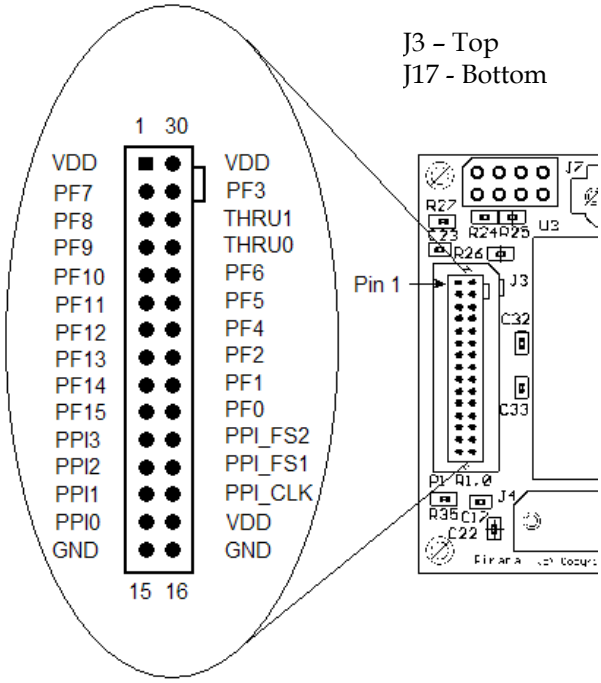


## 5.3 P1 Video Expansion Port

The Video Expansion Port (J3, J17) is connected to the Blackfin's general purpose parallel port (PF0..15, PPI0..3) providing a video and still imaging expansion option for a number of video camera daughter cards that support the SOC Robotics Video Bus standard(SVB). The SVB is a digital video bus interface standard supported by all SOC Robotics Video Camera Modules. The interface can also operate as a general purpose, bi-directional, high-speed digital interface port. There are two connectors – the top connector is a Samtec TFM-115F female 30 pin connector with 0.05in pin spacing. The top connector allows vertical mounting of video input cards. The bottom connector is a Hirose DF9-31 female 31 pin connector with 1mm pin spacing. The bottom connector is the same height and family as the Memory, Peripheral and AVR expansion bus connectors to ensure compatible motherboard and/or daughter card expansion options.

The video clock operates at the maximum speed of the Blackfin SCLK - 15ns period or 66MHz.

*Figure 5-4.* **J3/J17 – Video Expansion Port – Blackfin**



## 5.4 P1 Blackfin Memory and Peripheral Expansion Bus

The P1 Memory Expansion Bus (J4, J9) contains the address, data, read/write and two chip select lines of the Blackfin processor. The Peripheral Expansion Bus (J6, J7) contains the two high speed SPORT serial ports, bus arbitration lines and two chip select lines.

*Figure 5-5.* **J9 (Top) - Blackfin Memory Expansion Bus (Bottom –J4)**

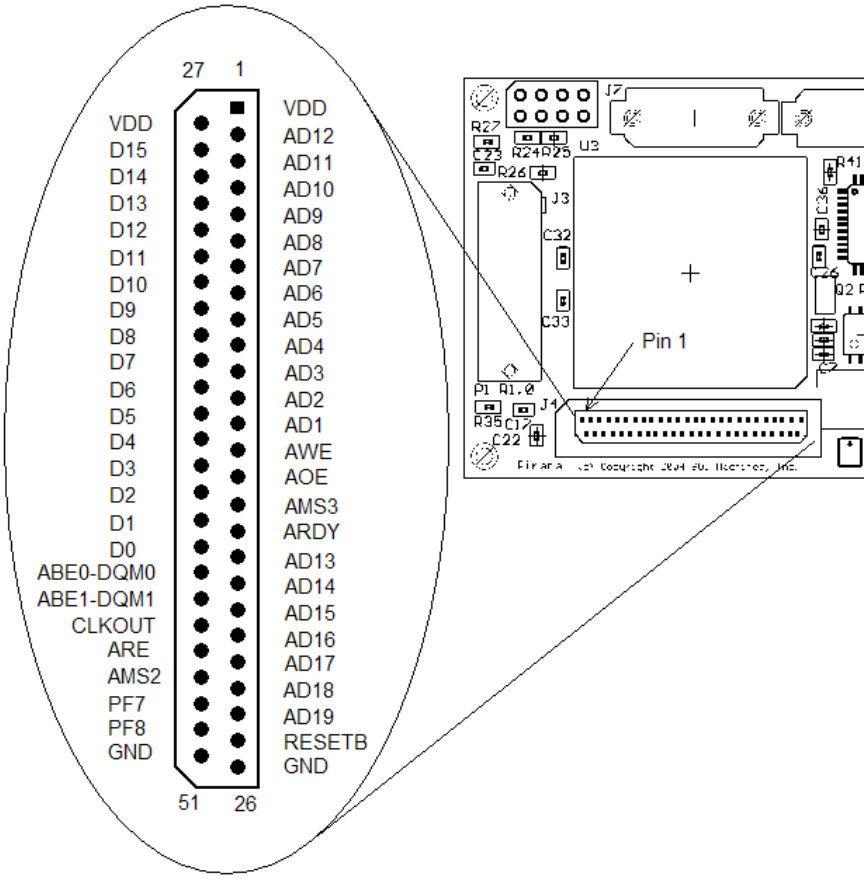
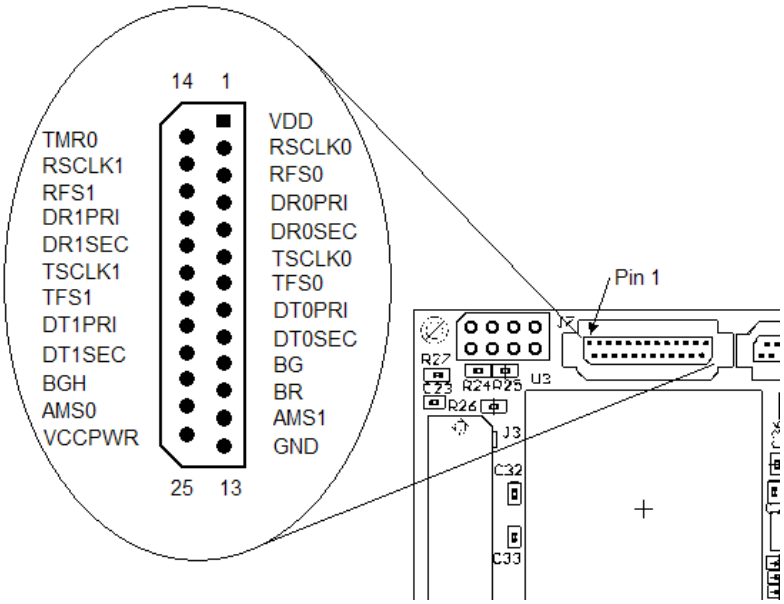


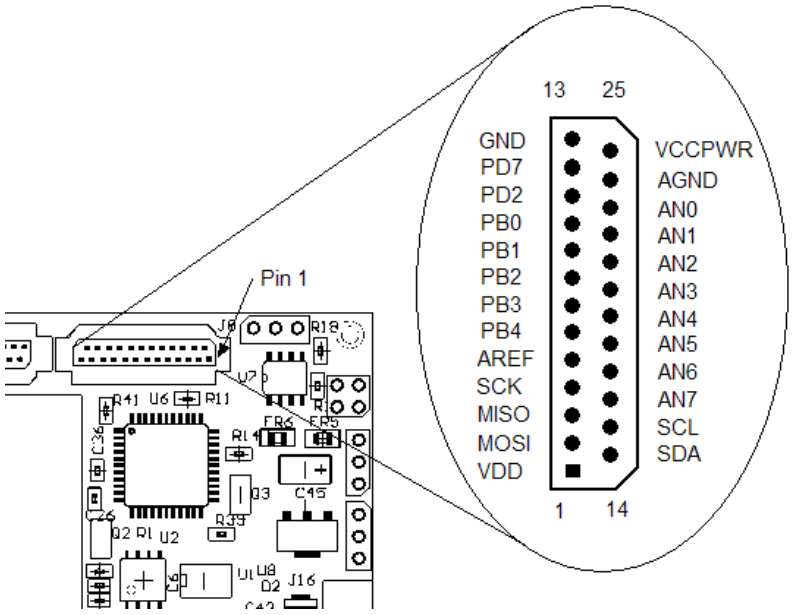
*Figure 5-6.* **J6 (Top) – Blackfin SPORT Expansion Port (Bottom – J7)**




## 5.5 AVR Expansion Port

The P1 AVR expansion bus connects the AVR 8 channel 10 bit analog port plus analog ground and AREF, 7 digital IO lines, SPI port and 2-Wire port to connector J5 on the top and J8 on the bottom.

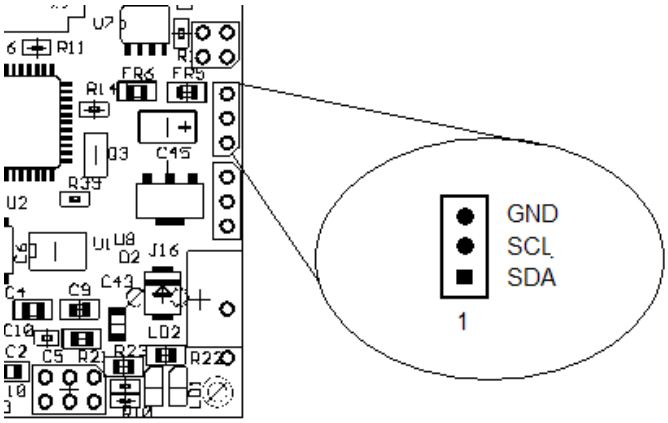
*Figure 5-7.* **J5 (Top) – AVR I/O Expansion Bus (Bottom –J8)**



## 5.6 TWI Port

The TWI Port is a smart, high-speed (400Kps), party line, half duplex communications bus controlled by the AVR. 2-Wire devices support remote wake-up, ID detection and broadcast operation.

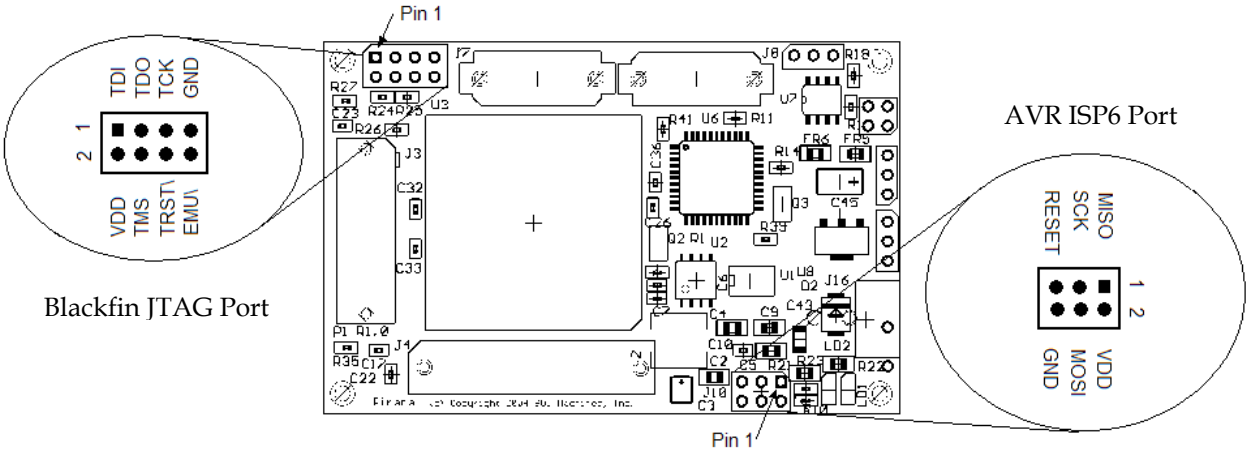
*Figure 5-8.* **J12 – AVR TWI Communication Port**




## 5.7 Programming Connectors – JTAG and ISP

The P1 has two programming/emulation connectors – an 8 pin JTAG connector for Blackfin emulation and a 6 pin ISP connector for AVR programming. The Blackfin JTAG connector is not pin compatible with the standard Analog Devices 14 pin Blackfin JTAG connector – an adapter is available to convert the 8 pin connector to a 14 pin connector. The AVR 6 pin connector is compatible with the Atmel 6 pin ISP connector pin out.

*Figure 5-9.* **J14 - Blackfin JTAG Port and J10 – AVR ISP Port**



## 5.8 P1 Input Power Connector Options

The P1 supports three different input power connector options. The default connector is a 2.5mm DC Jack SMT connector mounted on the bottom side of the board. The other two connector options are installed at the factory at time of purchase.

*Figure 5-10.* **J15 – P1 DC In 2.5mm Power Connector**

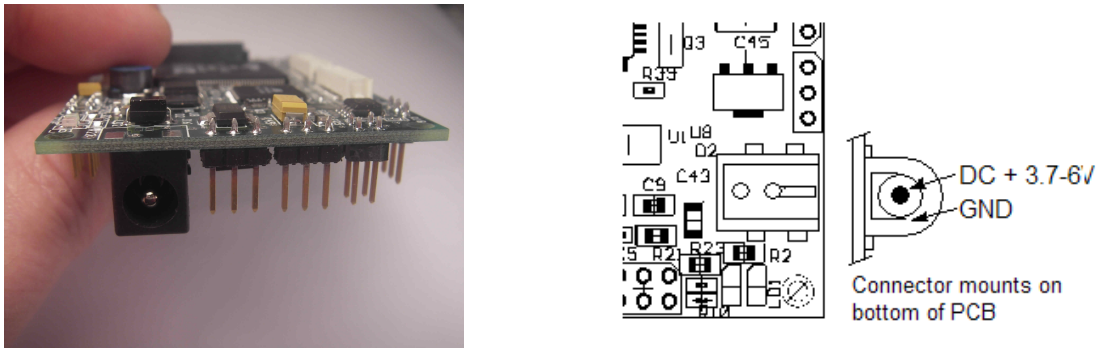



*Figure 5-11.* **J16 – P1 DC In Molex 13-555 SMT Power Connector (optional)**

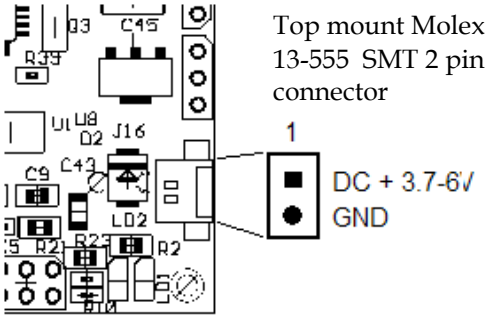
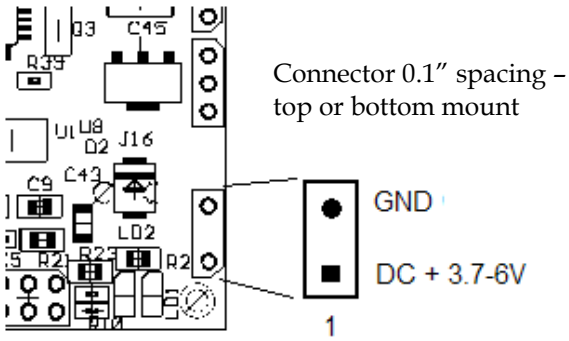



*Figure 5-12.* **J14 - P1 DC In Pin Power Connector (optional)**



# 6.0 Electrical and Mechanical Description

## 6.1 Component Layout

*Figure 6-1.* **P1 Top Component Layout**

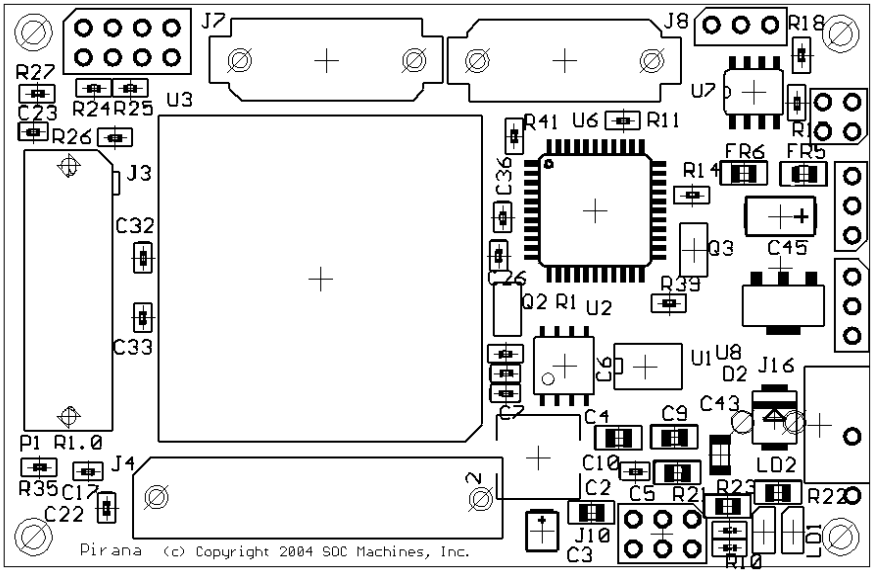
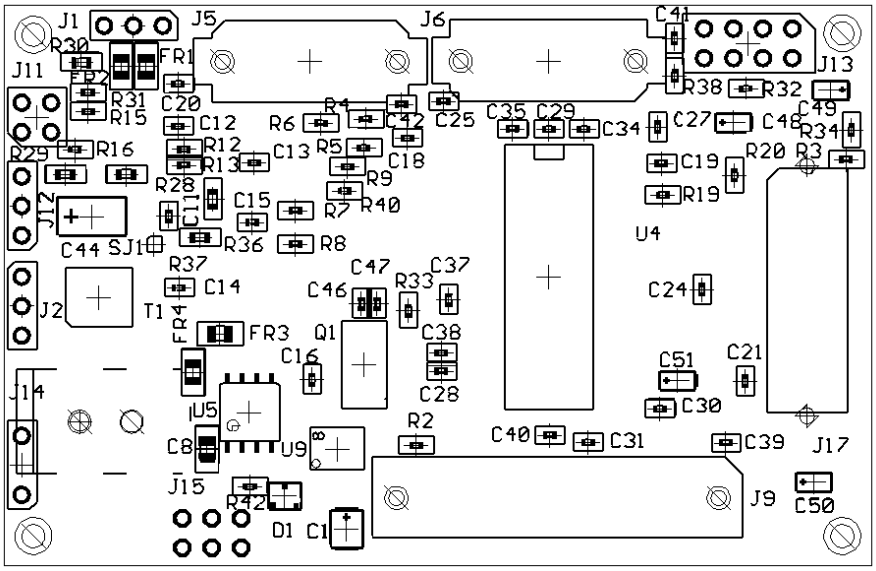



*Figure 6-2.* **P1 Bottom Component Layout**



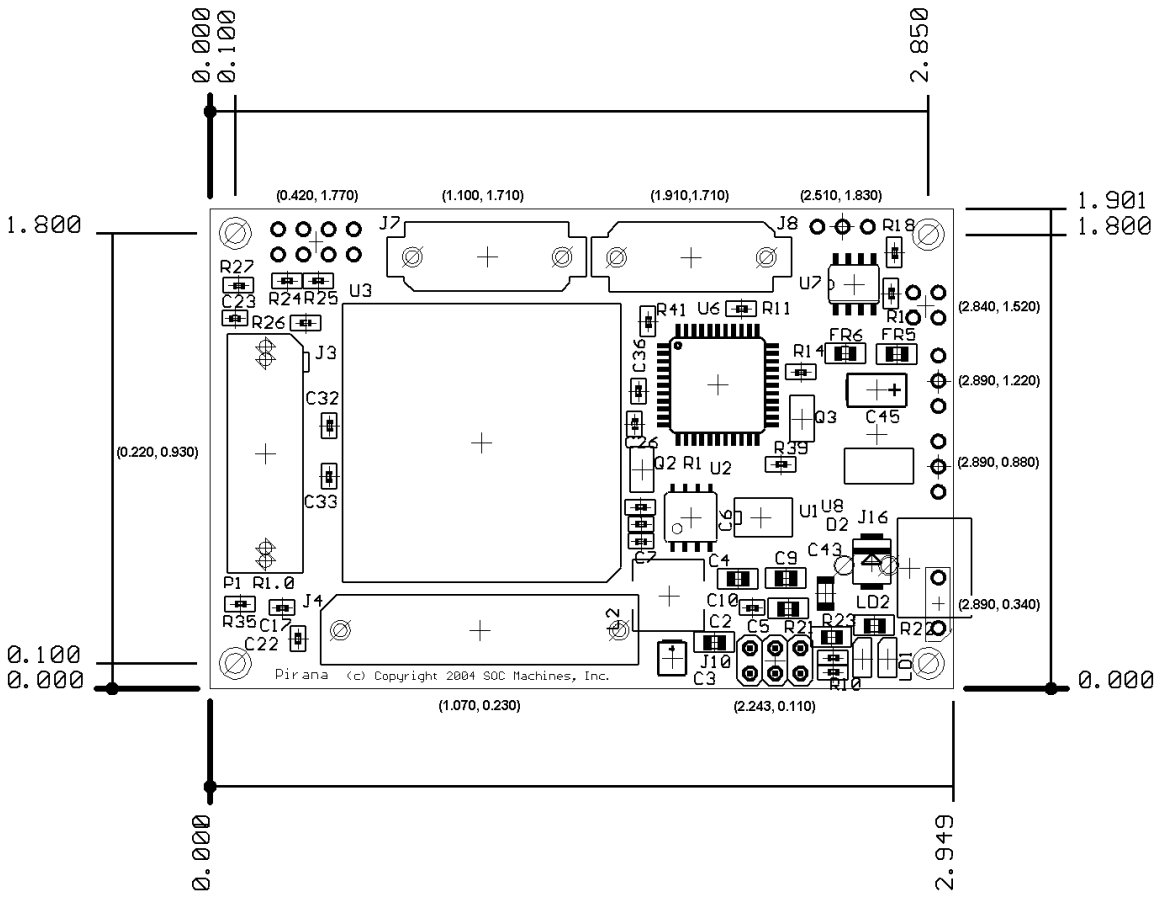
## 6.2 Electrical Specifications

The P1 input voltage must be in the range 4.3 to 7.0 volts DC. Do not exceed the 7.0 V limit or damage to the LDO regulator may result. LDO drops approximately 100mv at 200ma but there is an additional voltage drop through the reverse polarity diode. The LDO is designed to handle 1.5A although thermal constraints may limit maximum current to half this. The P1 nominal board voltage (VDD) is 3.3V. The Blackfin has an external voltage regulation circuit that generates 0.8 to 1.2VDC for the core. Core voltage level is under program control. The P1 consumes about 180ma at full speed the majority of which is consumed by the Blackfin when running at full speed. The AVR consumes less the 8ma. DC IN is reverse polarity protected. VDD and GND are routed to all expansion connectors. DC IN is routed to the Blackfin SPORT connectors and the AVR Expansion connector. The AVR analog inputs have a separate AGND plane for improved noise immunity.

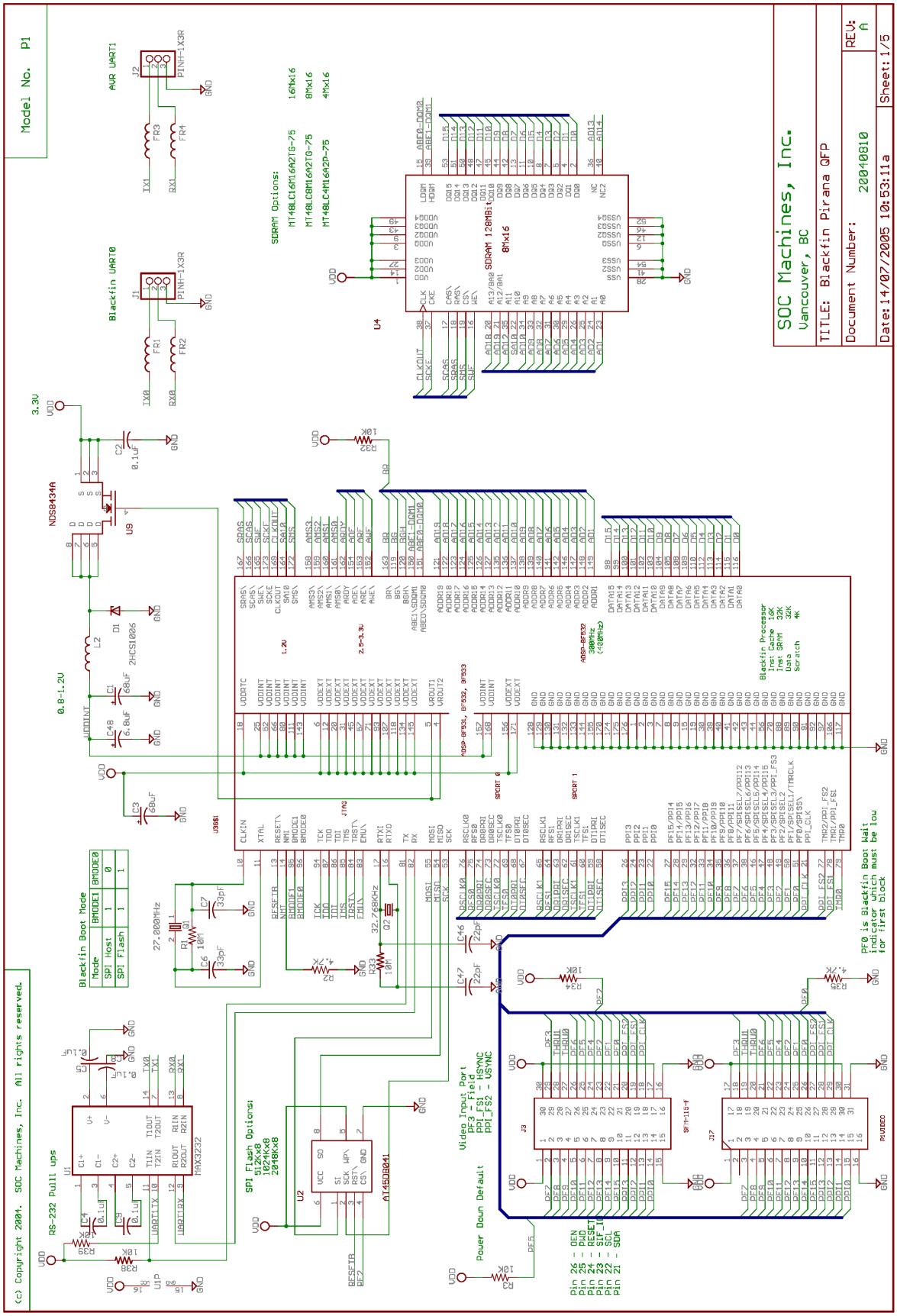
## 6.3 Mechanical Dimensions

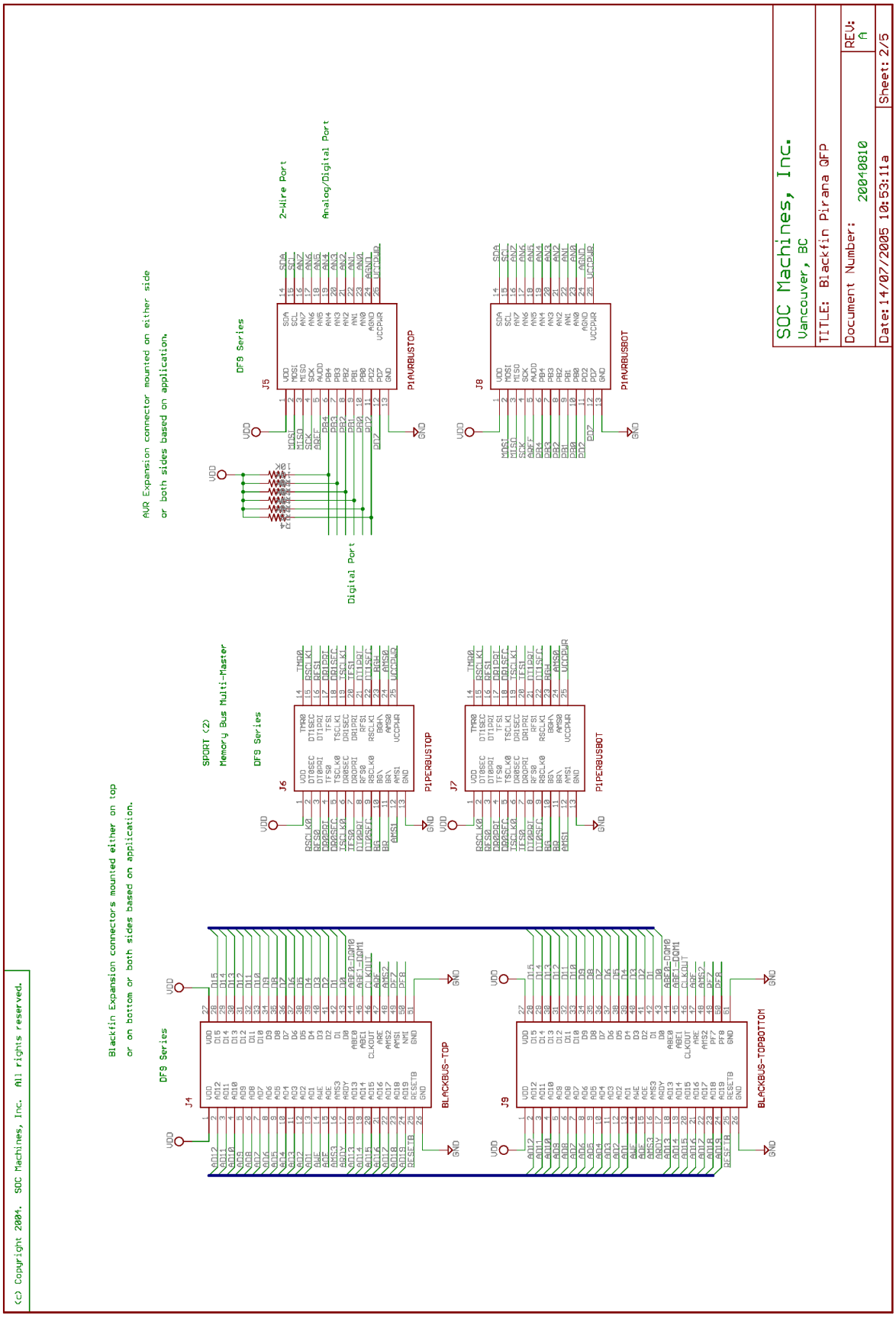
All board dimensions are in inches. Connector locations with respect to the lower left corner are included in the drawing. A sample schematic with connector library and board layout in Eagle CAD format is available at [www.soc-Robotics.com/download/p1layout.htm](www.soc-Robotics.com/download/p1layout.htm). Layouts for both top and bottom daughter cards is included in the ZIP file.

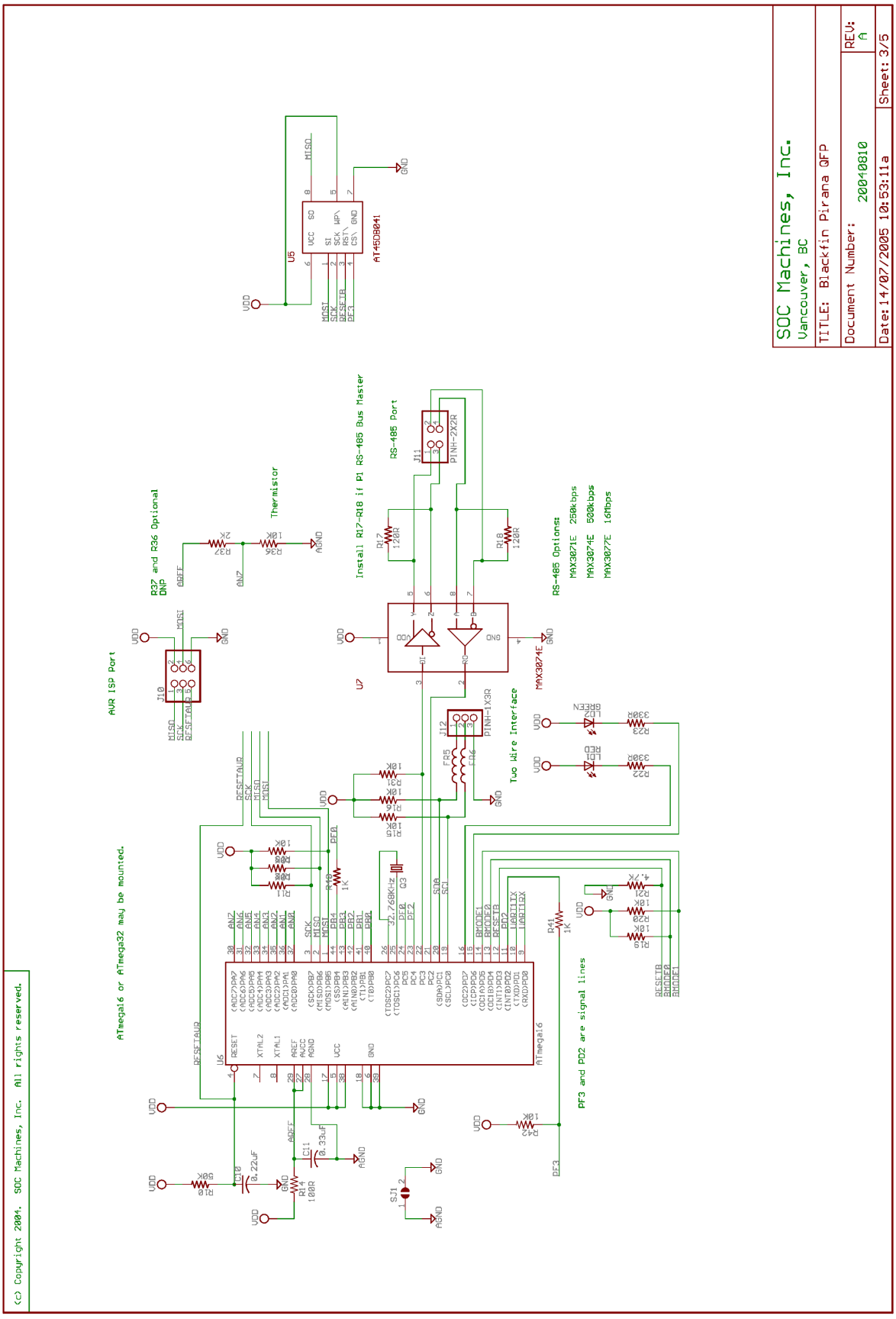
*Figure 6-3.* **P1 Mechanical mounting dimensions**



# P1 Circuit Schematics


Model No. P1
SOC Machines, Inc.
Vancouver, BC
TITLE: Blackfin Pirana QFP
Document Number: 20040810
REV: A
Date: 14/07/2005 10:53:11a
Sheet: 1/5
(c) Copyright 2004. SOC Machines, Inc. All rights reserved.
Blackfin Boot Mode
SPI Flash Options:
512Kx8
1024Kx8
2048Kx8
Video Input Port
PF3 Field
PPI_FS1 - HSYNC
PPI_FS2 - VSYNC
Power Down Default
PF0 is Blackfin Boot Wait indicator which must be low for first block
AVR UART1
Blackfin UART0
SDRAM Options:
MT48LC16M16A2TG-75 16Mx16
MT48LC8M16A2TG-75 8Mx16
MT48LC4M16A2P-75 4Mx16
SDRAM 128MBit 8Mx16
Blackfin Processor
Ins: Cache 16K
Ins: SRAM 32K
Data 32K
Scratch 4K
RS-232 Pull ups
MAX3232
AT45DB041
NDS9434A
3.3V
0.8-1.2V
2.5-3.3V
1.2V
27.000MHz
32.768KHz


(c) Copyright 2004. SOC Machines, Inc. All rights reserved.
Blackfin Expansion connectors mounted either on top
or on bottom or both sides based on application.
DF9 Series
J4
BLACKBUS-TOP
J9
BLACKBUS-TOPBOTTOM
SPORT (2)
Memory Bus Multi-Master
DF9 Series
J6
PIPEBUSTOP
J7
PIPEBUSBOT
AVR Expansion connector mounted on either side
or both sides based on application.
DF9 Series
J5
PIAVRBUSTOP
2-Wire Port
Analog/Digital Port
Digital Port
J8
PIAVRBUSBOT
SOC Machines, Inc.
Vancouver, BC
TITLE: Blackfin Pirana QFP
Document Number: 20040810
REV: A
Date:14/07/2005 10:53:11a
Sheet: 2/5


SOC Machines, Inc.
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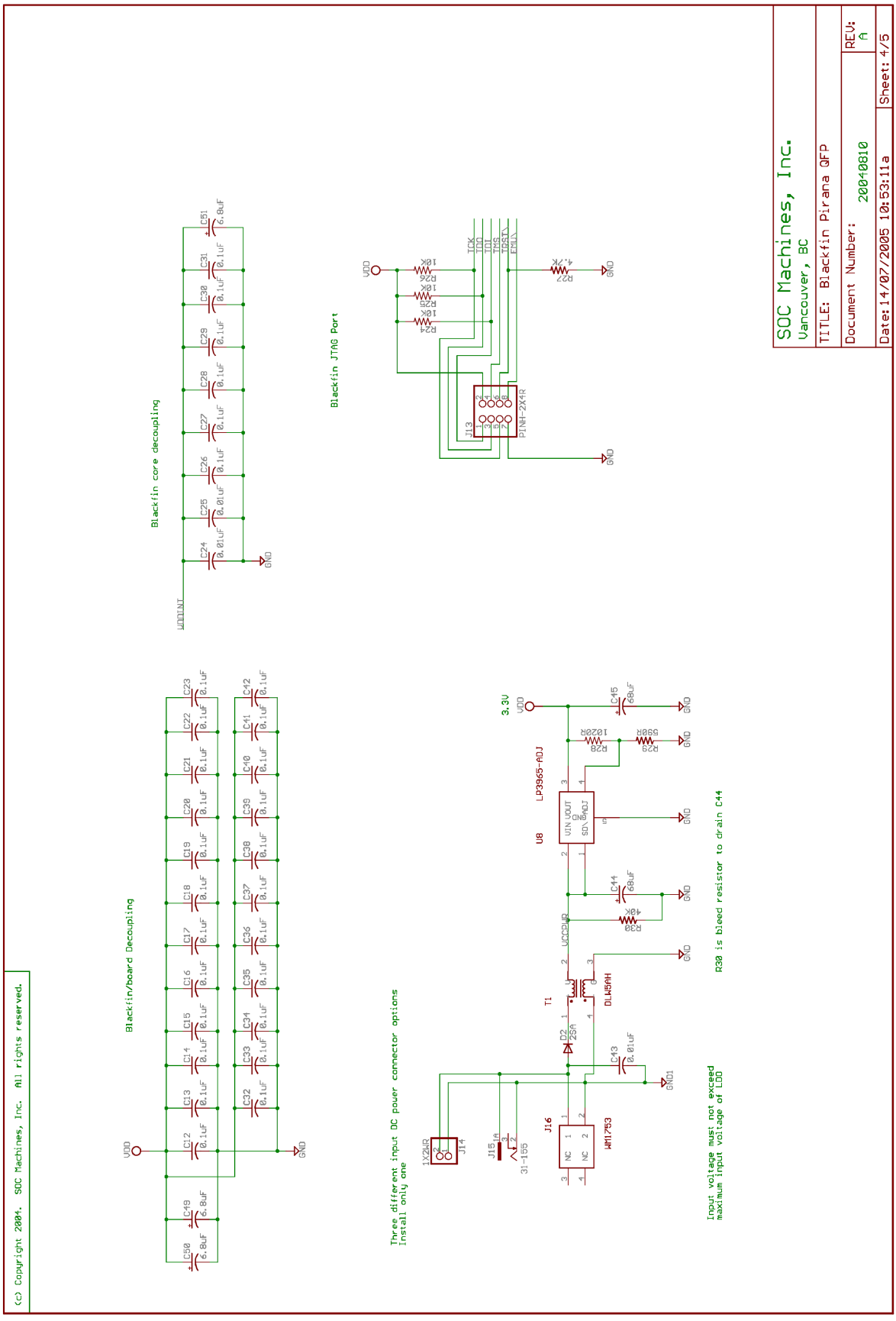
TITLE: Blackfin Pirana QFP
Document Number: 20040810
REV: A
Date: 14/07/2005 10:53:11a
Sheet: 3/5
(c) Copyright 2004. SOC Machines, Inc. All rights reserved.
ATmega16 or ATmega32 may be mounted.
AVR ISP Port
R37 and R36 Optional
DNP
Thermistor
Install R17-R18 if P1 RS-485 Bus Master
RS-485 Port
RS-485 Options:
MAX3071E 250Kbps
MAX3074E 500Kbps
MAX3077E 16Mbps
MAX3074E
Two Wire Interface
PF3 and PD2 are signal lines
ATmega16
AT45DB041



## Notes: